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ON THE INFLUENCE OF SPACE-QUANTIZATION EFFECTS ON THE RF NOISE BEHAVIOUR OF DG MOSFETS

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We present a particle-based Monte Carlo investigation of the high frequency noise behavior of a double gate MOSFET. The effective potential approach has been considered for the description of vertical quantum confinement of carriers within the channel. The intrinsic noise sources and the main circuital noise parameters are studied, together with the static and dynamic parameters, thus allowing to provide a full comprehension of the inner physics of the device and elucidating the consequences of quantum mechanical space-quantization effects (like charge repulsion from the gate-oxide boundaries). Results show that neglecting quantum phenomena leads to an important overestimation of gate capacitance and device transconductance and an underestimation of the final influence of induced gate noise (via the normalized parameter R) on the circuital noise parameters at RF and microwave frequency ranges.

Keywords: Double Gate MOSFET; ensemble Monte Carlo; effective potential; high-frequency noise.

1. Introduction

The downscaling of the bulk Silicon MOSFET transistor has been the key of the progress of semiconductor technologies in the last 30 years. However, if the continuation of the ITRS roadmap is desired (predicting operative MOSFET devices in production lines with physical gate-lengths of 7 nm by 2018 [1]), an extraordinary effort must be devoted to avoid the severe short-channel effects appearing in ultra-scaled devices [2]. Double Gate (DG) MOSFETs show particular interest for this purpose. Parasitics represent still a very important constraint for these devices; however, if this problem is overcomed, DG MOSFETs will become a privileged alternative to conventional devices due to their almost ideal intrinsic MOSFET behavior [3]. The analysis of the dynamic and noise behavior of these devices is thus a mandatory issue. The ensemble Monte Carlo (EMC) method is an excellent approach to this end [4].

Quantum effects in devices with extremely small dimensions like DG MOSFETs may play a significant role that can not be avoided in reliable studies. The active layer

thickness in these devices can be smaller than 10 nm, and vertical channel quantization represents the main concern [5]. The self-consistent solution of the Schrödinger and Poisson equations, which should be the most feasible approach, has shown difficulties to be implemented in EMC simulators with an acceptable computational cost [6]. Quantum corrections to the potential (based on the second derivative of the square root of local density, also known as *density-gradient approach*) have become a usual solution to compute quantum effects in the channel of MOSFETs [7]. Recently, a more generalized approach has been proposed, the *effective potential* [8], which allows reproducing the main space-quantization effects occurring in ultra-small devices. In spite of the efforts developed by many authors in the EMC simulation of bulk and SOI devices [6, 9, 10], there is still a lack of studies on the consequences of such an approaches when dealing with high-frequency dynamic and noise behavior of the transistors.

The aim of this work is to analyze the influence of space-charge quantization in the channel of a DG n-MOSFET by means of a particle-based Monte Carlo simulator. In Sec. 2.1, the topology of the structure under analysis, together with the main features of the Monte Carlo simulator, is presented. Results for the internal quantities of interest are discussed in Sec. 3.1. The most significant high frequency small-signal equivalent circuit parameters are analyzed in Sec. 3.2, and the noise performance is investigated in Sec. 3.3. Finally, the main conclusions of the work are drawn.

2. Simulated Structure and Monte Carlo Procedure

2.1. *Simulated structure*

Figure 1 shows a scheme of the DG n-MOSFET studied in this work. The topology chosen reproduces the main features of this type of devices, and it is similar to other ideal ensemble Monte Carlo DG structures found in the literature [11]. Between the symmetrical gates and a gate oxide of 2 nm, transport takes place within a Silicon film of 5 nm. The gate length is 50 nm, and the doping concentration in the channel is $2 \cdot 10^{18}$ cm^{-3} (although the main benefits of DG technology are obtained when undoped channels are used, in real devices it is a common practice to use doped channels to avoid negative threshold voltages [3]). The workfunction of the metal gate is 4.17 eV. The regions close to the source and drain terminals have a doping concentration of 10^{19} cm^{-3}.

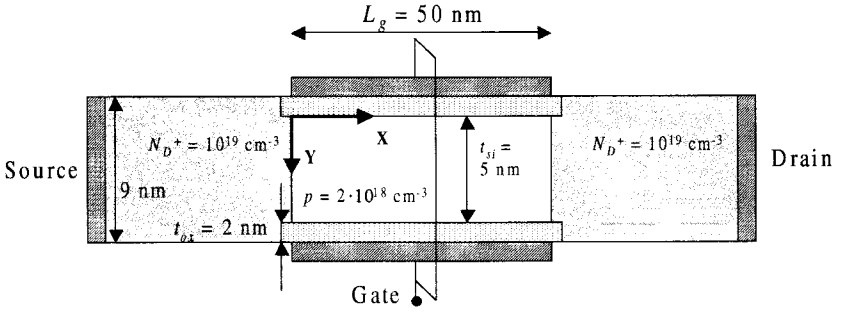

Fig. 1. Scheme of the simulated device.

2.2. *Monte Carlo procedure*

Numerical calculations were performed by means of an ensemble bipolar Monte Carlo simulator [4] self-consistently coupled with a two-dimensional Poisson solver. The simu-

lator was successfully employed in previous works for the study of different kinds of transistors and experimental deep-submicron Silicon devices [12, 13]. However, it must be noticed that in those works space-quantization effects were disregarded due to the topologies of the devices under study: a semiclassical model in which carriers are considered as point charges in real space was taken into account.

In the present work, due to the importance of vertical confinement within the channel of DG MOSFETs we chose the effective potential approach [8]. After solving Poisson equation at each timestep, a convolution of the local potential with the Gaussian function associated to the size of the electron wave packet is performed in order to evaluate the effective potential (V_{eff}), from which the electric fields to be used in the Monte Carlo kernel are derived [8]:

$$Veff(x,y) = \frac{1}{\sqrt{2\pi}\sigma}\int V(x,y')\exp\left(-\frac{(y-y')^2}{2\sigma^2}\right)dy' \qquad (1)$$

where σ is the standard deviation for the Gaussian function. In the absence of experimental data to fit this parameter, we chose a value of 0.5 nm following the value reported in [9] for a MOSFET device.

3. Results

3.1. *Static characteristics*

Figure 2(a) shows the results obtained for the transfer characteristic at $V_{DS} = 0.75$ V when considering the effective potential (black symbols) and those obtained in a completely semiclassical framework (white symbols). As it can be observed, when considering the effective potential approach a progressive reduction of the drain current is obtained as V_{GS} is increased (around 15% for the highest V_{GS}), which is in good agreement with the results shown by other authors in thin SOI devices [6].

Figure 2(b) shows the results obtained for the "classical" Poisson potential (dashed black line) and the effective potential (solid black line), along the Y axis at the middle of the gate for $V_{GS} = 0.375$ V and $V_{DS} = 0.0$ V. In the case of the classical potential, sharp barriers corresponding to the oxide-semiconductor interfaces are observed. Due to the presence of the second gate at the bottom of the active layer, the conduction band within the channel is quite flat, with the minimum of the potential located exactly at the Si-SiO_2 interfaces. However, when considering the convolution of the Poisson potential with the Gaussian function some differences are observed. A much softened potential profile is obtained in the vicinity of the oxide-semiconductor surfaces (solid black line). As a consequence, a strong vertical (Y direction) electric field repelling electrons towards the middle of the channel appears. In contrast with other SOI or MOS structures [6, 10], we have not observed a significant shift of the minimum value of the potential as compared to the classical case. Since longitudinal quantization was not considered in this work, electric fields along the X direction did not show relevant differences.

Regarding the electron concentration (grey lines in Fig. 2[b]), when dealing with a completely semiclassical approach two inversion layers are obtained just adjacent to the semiconductor-oxide interfaces, as it is expected from the potential profile. Even in this case, the proximity of both inversion layers leads to a significant concentration of carriers at the middle of the channel, which in fact shows a volume inversion regime, as pointed out by other authors [6]. However, when the effective potential approach is considered, the maximum values of the concentration profile are displaced around 1.5 nm from the

$Si\text{-}SiO_2$ interfaces (which are practically depleted of inversion carriers due to the repelling electric field in the Y direction), and the concentration at the middle of the channel is readily augmented. However, if we calculate the total carrier sheet density along the channel, vertical quantization induces a reduction of the total inversion population in the active area. As a consequence, a lower value of the saturation drain current is provided by the effective potential approach as compared to the classical potential calculation, which is in good agreement with the results obtained by other authors in other MOSFET devices [6, 14]. It is necessary to mention that, according to the work by Palestri *et al.* [15], the V_{eff} approach is able to reproduce accurately the total inversion charge, but at the same time it can overestimate the shift of carrier concentration from the interface as compared to more rigorous solutions of Schrödinger and Poisson equations. Consequently, the concentration profile and the gate-to-source capacitance could be not exactly determined. A tailored combination of the oxide barrier height and the σ parameter for the different bias conditions could provide more accurate results. However, in the absence of static and dynamic experimental measurements, we have chosen a unique set of values for the above-mentioned parameters.

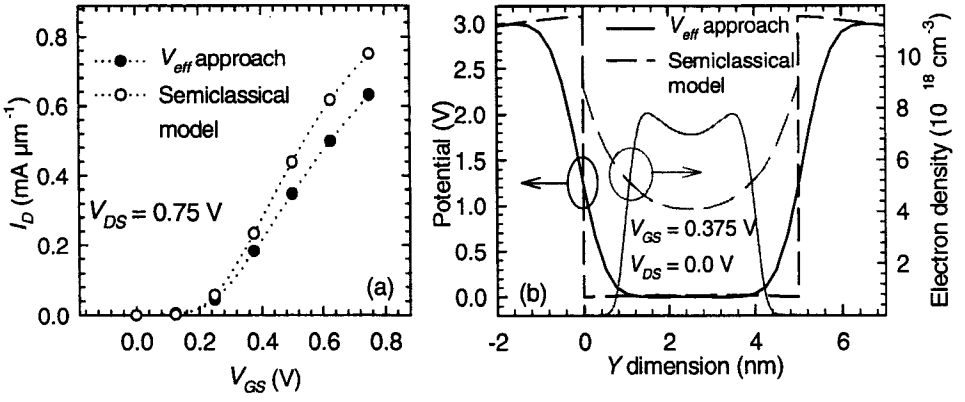

Fig. 2. (a) I_D-V_{GS} transfer characteristic for V_{DS} = 0.75 V and (b) potential (black lines) and concentration (grey lines) at the middle of the channel for V_{GS} = 0.375 V and V_{DS} = 0.0 V.

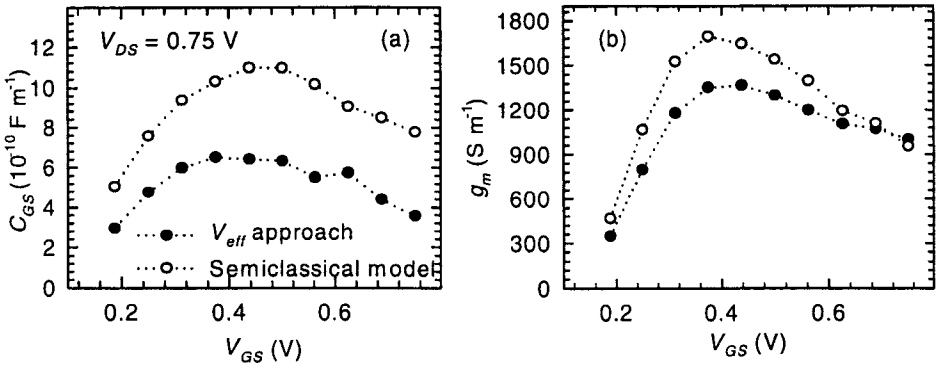

Fig. 3. Values for (a) C_{GS} and (b) g_m as a function of V_{GS} in saturation (V_{DS} = 0.75 V).

3.2. *High frequency dynamic behavior*

The parameters of the small-signal equivalent circuit (SSEC) of the DG MOSFET have been found to be frequency independent at least up to 50 GHz. We report here the main differences found between the semiclassical and effective potential approaches. Regarding the SSEC capacitances, the main changes originated by the consideration of the effective potential take place for the gate-to-source capacitance C_{GS}, shown in Fig. 3(a), which is noticeably reduced, thus indicating a loss of gate control over the charge in the channel. The charge set-back from the oxide interfaces produced by the vertical potential well would be equivalent to considering a thicker gate oxide: consequently, the oxide capacitance would decrease and so does the gate capacitance, in good agreement with the results obtained by other authors when investigating space-quantization phenomena in MOS capacitors [16]. Lower values of g_m are also obtained with the effective potential approximation, Fig. 3(b), like found by other authors in ultra-thin SOI devices [6] and FIBMOS transistors [14]. It can be concluded that semiclassical models yield an overestimation of the current drive capability of ultra-small devices due to the increased inversion charge in the channel. As a consequence of the behavior described for g_m and C_{GS}, we have checked that disregarding space-quantization leads to reduced maximum values for the cut-off frequency (260 GHz) as compared to the values provided when V_{eff} is considered (315 GHz) due to the substantial decrease of C_{GS} observed in this latter case and the comparatively minor reduction of g_m.

3.3. *Noise results*

To analyze the noise behavior of the transistor we use the usual two-port device representation, with two noise current generators (calculated from current fluctuations in the Monte Carlo simulation), one at the input, S_{IG}, and other at the output, S_{ID}, both correlated (S_{IGID}) [17]. The calculated spectral densities of current fluctuations show (both for V_{eff} and semiclassical approaches) the usual frequency dependence found in FET devices in the RF domain [17]: S_{ID} exhibits a white noise behavior, S_{IG} has an f^2 dependence and the imaginary part of S_{IGID} depends linearly on f; the real part of S_{IGID} can be neglected as compared to the other quantities. In the main discussion of this section we shall focus on the study of the bias dependence of the noise parameters (that may provide information about the importance of space-quantization phenomena) and results will be shown for a given frequency.

In Fig. 4, the results for (a) S_{ID} and (b) S_{IG} are shown as a function of the gate voltage for $V_{DS} = 0.75$ V (circles), together with the results for those same quantities as a function of drain voltage at $V_{GS} = 0.375$ V (triangles). The slight deviations from the monotonic behavior found in some points (which is usual in noise Monte Carlo calculations) are due to numerical errors; however, the tendencies remain unambiguous along the whole bias range. An increase of S_{ID} with V_{GS} is observed when using both approaches, in good agreement with the bias dependence for this same quantity obtained in other MOSFET devices [13]. Neglecting the vertical confinement of carriers yields to a general overestimation of this quantity in saturation (for V_{GS} larger than 0.5 V and the lowest values of V_{DS} in Fig. 4(a) the device approaches or indeed operates in the triode regime). When dealing with S_{IG}, little differences are observed in saturation [Fig. 4(b)]; however, for a fixed V_{GS} [triangles in Fig. 4(b)], in the triode region an underestimation of this quantity is provided by the semiclassical approach.

In order to provide a more a comprehensible and accurate picture of the high-frequency noise, it is necessary to use normalized parameters that relate the intrinsic

noise sources to the dynamic behavior of the device. For this purpose, the frequency independent P, R and C parameters are usually employed [17]. P is the diffusion noise parameter related to current fluctuations at the drain, R is associated to the induced gate noise and C is the normalized correlation coefficient between both current noise generators. The results obtained in our simulation for these parameters are shown in Fig. 5 as a function of the gate voltage. In the case of P, no significant changes take place. However, important differences for R (that is the normalization of S_{IG} by the gate capacitance via the admittance parameter Y_{11}) are observed: when considering the effective potential, a much higher value is obtained. Although at fixed V_{DS} the noise at the gate is similar for both approaches [Fig. 4(b)], in the effective potential case it develops by means of a much lower dynamic capacitive coupling (lower C_{GS}). Therefore, when space-quantization effects are considered, the final influence of induced gate noise in terms of R is amplified, while semiclassical models may provide an incorrect description of this parameter.

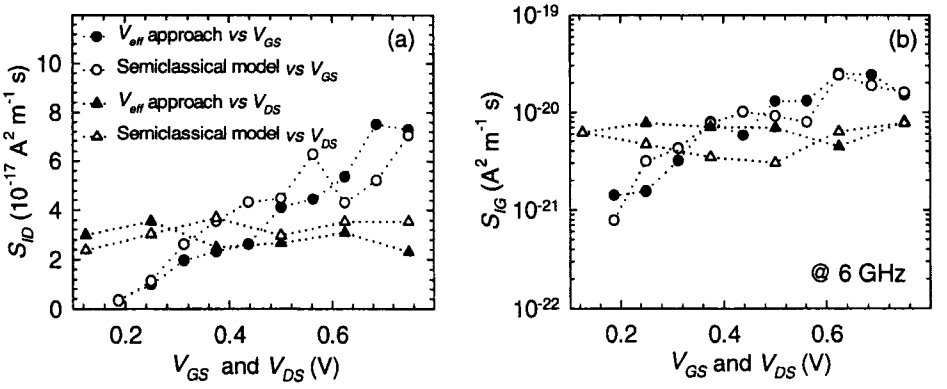

Fig. 4. Values of (a) S_{ID} and (b) S_{IG} at 6 GHz as a function of V_{GS} in saturation (circles, V_{DS} = 0.75 V), and as a function of V_{DS} (triangles, V_{GS} = 0.375 V).

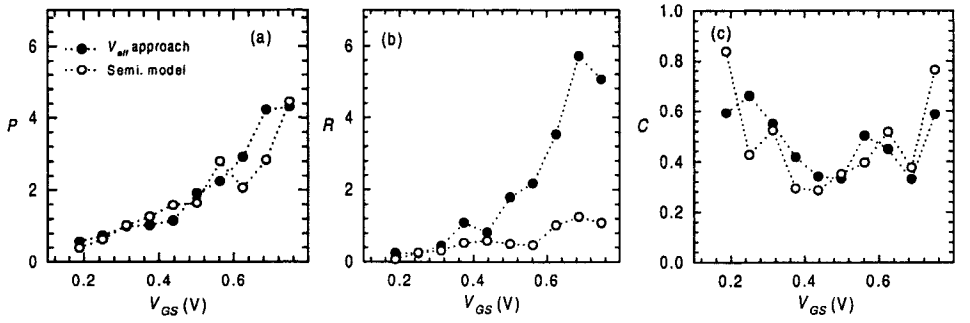

Fig. 5. (a) P, (b) R and (c) C noise parameters as a function of gate voltage.

Regarding the correlation factor C, the highest values are obtained at low V_{GS} when the effective potential is not taken into account. It is also noticeable that in both cases the results are in general higher than the predicted values for a theoretical long-channel MOSFET, this is, 0.4 [17], thus indicating an important correlation between drain current

fluctuations and induced gate noise in DG MOSFETs, and thus showing the signature of quasi-ballistic transport in these structures.

Once the intrinsic noise parameters have been analyzed, the calculation of the usual four noise parameters used in circuit design (minimum noise figure NF_{min}, equivalent noise resistance R_n, phase and module of optimum reflection coefficient Γ_{opt}) is performed by means of the procedure described in [18]. The results are shown in Fig. 6. In general, extremely reduced values of NF_{min} are obtained with both approaches, thus indicating the excellent intrinsic behavior of the DG MOSFET. It must be remarked that no extrinsic elements where taken into account in the results presented in this work. The parasitic access resistances (which can be important in this type of devices) would produce worse values of this figure of merit in a fabricated device. Regarding the influence of space-quantization effects, it can be observed how the minimum noise figure is raised at high V_{GS} (larger than 0.5 V) when computing the effective potential. This can be attributed to the higher influence of the induced gate noise parameter R in this case (significantly amplified by the small-signal gate capacitance), which is significantly underestimated by classical models as discussed in the previous paragraph.

Semiclassical calculations provide lower values for the equivalent noise resistance R_n. Since this parameter is directly depending on the S_{ID}-to-g_m^2 ratio, we may conclude that the higher transconductance provided by this approach is the main responsible for the lower values of R_n. Space-quantization yields therefore to a more critical condition to achieve the best device noise performance operating in the high-frequency regime. This is a delicate condition where semiclassical models could predict a non-realistic low-noise performance. The optimum complex reflection coefficient Γ_{opt} does not show worthmentioning differences between both approaches, with the only exception of a very small increase of the phase if space-quantization is neglected.

Finally, it is necessary to mention that the paramount complexity of quantum phenomena (affecting the band structure and scattering mechanisms) in such small devices may provide additional differences to those observed in the present work in the high-frequency noise results obtained with quantum and semiclassical models.

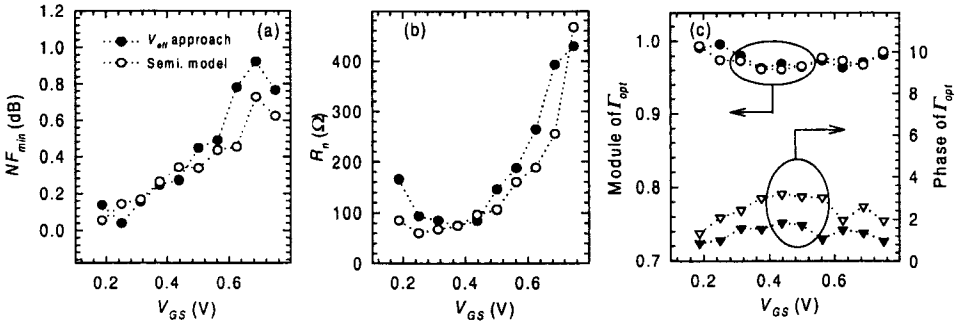

Fig. 6. (a) Minimum noise figure NF_{min}, (b) equivalent noise resistance R_n and (c) module and phase of Γ_{opt} as a function of V_{GS} at V_{DS} = 0.75 V and a frequency of 10 GHz.

4. Conclusions

We have performed an EMC investigation of space-quantization effects on the static, dynamic and high-frequency noise behavior of a DG MOSFET. For this purpose, the

effective potential approach has been implemented in a semiclassical Monte Carlo kernel. The smoothing of the potential profile generated by the consideration of the electron wave packet results in a set-back of electrons from the Si-SiO_2 interfaces and a total minor inversion charge inside the channel. As a consequence, a reduced gate capacitance and transconductance are obtained as compared to the results provided by a completely semiclassical model. Although not significantly affecting the intrinsic gate noise source, the important modification of small-signal ac parameters yields a steady augmentation of the induced gate noise factor R when the effective potential approach is considered, thus leading to worse noise figures of merit (NF_{min}, R_n) than in the case of neglecting quantum effects.

Using semiclassical models for DG devices with extremely thin active layers may provide an overestimation of the high-frequency noise performance. Models dealing with space-quantization effects should be considered in order to provide a more accurate and realistic description of the high-frequency noise behavior. Therefore, complex physical models (probably beyond the effective potential approach) able to provide a complete and detailed treatment of the influence of quantum confinement on the device noise are to be developed for their use in EMC simulators in a proper and computationally acceptable way.

Acknowledgments

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