Fabrication and fundamentals of operation of an InAlAs/InGaAs velocity modulation transistor

Nicolas Wichmann,[1,a)] Beatriz G. Vasallo,[2] Sylvain Bollaert,[1] Yannick Roelens,[1] Xavier Wallart,[1] Alain Cappy,[1] Tomás González,[2] Daniel Pardo,[2] and Javier Mateos[2]
[1]*Institut d'Électronique de Microélectronique et de Nanotechnologie (IEMN), UMR CNRS 8520 Avenue Poincaré, BP60069, 59652 Villeneuve d'Ascq Cedex, France*
[2]*Dpto. de Física Aplicada, Universidad de Salamanca, Plaza de la Merced s/n, 37008 Salamanca, Spain*

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We report the design, fabrication, and characterization of an InP-based InAlAs/InGaAs velocity modulation transistor (VMT) based on the double-gate high electron mobility transistor topology. When electrons are transferred between two channels with different mobility, the drain current is modulated while keeping the total carrier density constant. For the fabrication of the transistor, the epitaxial growth has been optimized in order to accomplish the maximum mobility difference between the two active channels. DC characteristics of our VMT have been extracted and an ensemble Monte Carlo simulator is employed to study the microscopic behavior of the fabricated device. The numerical analysis of the carrier density and velocity variation with the gate bias in differential mode demonstrates the actual velocity modulation operation of the fabricated transistors. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3095482]

To further improve the high-frequency and low-noise behavior of InP-based high electron mobility transistors (HEMTs), alternative solutions based on an evolution of the standard topology have been proposed. Thus, the double-gate (DG) HEMT, a HEMT with two gates placed on each side of the conducting InGaAs channel, has been recently developed.[1–5] The progress of the DG-HEMT technology allows the design and fabrication of InP-based velocity modulation transistors (VMTs). The concept of VMT was proposed by Sakaki[6] in 1982 and the first transistor was realized by Cohen *et al.*[7] in 1997 on a GaAs/AlGaAs heterostructure. These devices employ the modulation of the carrier velocity to vary the drain current I_D in order to overcome the limit on the electron transit time observed on standard field effect transistor. To achieve that, the source and drain electrodes are connected by two channels with different mobility μ and two gates control the amount of electrons in the channels N_T. Electrons can be shifted between the two channels by changing the gate voltages in differential mode. Due to the different transport properties in the two channels, the modulation of I_D can be effective while keeping N_T constant. Because of the very low capacitive effect associated to this current control, high cutoff frequencies can be expected.

In this work, the technological process and the DC electrical characterization of a 100-nm-gate length InAlAs/InGaAs VMT are presented. Since the local carrier density in the fabricated devices cannot be extracted experimentally, the velocity modulation of I_D is demonstrated by means of a two-dimensional (2D) *ensemble* Monte Carlo (MC) simulator. This model, whose validity has been checked for standard[8,9] and DG-HEMTs,[4,5] provides a full microscopic interpretation of the fundamentals of the velocity modulation operation of the VMT.

Lattice matched InAlAs/InGaAs VMT epilayers are grown by gas source molecular beam epitaxy (Riber 32P) on InP substrate. The initial epitaxial layer structure, very similar to two single HEMT layer structures, is analogous to that of the DG-HEMT reported in previous works.[1–3] A 200 nm thick InGaAs and a 100 nm thick InP etch-stop layer, which served to remove the InP substrate by wet chemical etching, are first deposited. Then, the actual active layers are grown: a 10 nm thick InGaAs Si-doped (6×10^{18} cm^{-3}) first cap layer, a 12 nm thick first InAlAs Schottky contact layer, a Si-δ-doping plane (5×10^{12} cm^{-2}), a 5 nm thick InAlAs first spacer layer, and a 20 nm thick undoped InGaAs high-mobility μ channel. Then, a 20 nm thick doped InGaAs low-μ channel is grown with both silicon (N-type) and beryllium (P-type) dopants with a concentration of 10^{18} cm^{-3}. The compensated-doping channel layer allows increasing the ionized impurity scattering and thus decreasing the electron mobility. In this way, an important velocity modulation between the two channels takes place while avoiding differences in the electron concentration between them at thermal equilibrium. Finally, a 2 nm thick undoped InAlAs second spacer layer, a second Si-δ-doping plane (4×10^{12} cm^{-2}), a 15 nm thick InAlAs second Schottky layer, and a 10 nm thick second cap layer are grown. The mobilities of the high-μ and low-μ channels at room temperature measured by Hall effect on test structures are 10 000 and 2600 cm^2/V s, respectively.

The VMT fabrication process is very similar to that of the DG-HEMT. Mesa structures are defined by photolithography and wet chemical etching. The source and drain Ohmic contacts are fabricated by using alloyed Ni/Ge/Au/Ni/Au. Bonding pads are fabricated by evaporating Ti/Pt/Au/Ti. The last titanium layer is necessary to improve the adhesion of the benzocyclobutene (BCB) polymer to the bonding pads during the wafer transfer process. The first 100 nm T-shape gate is then fabricated by e-beam lithography using a conventional PMMA/P(MMA-MAA) bilayer resist process. The first gate-recess process is carried out by wet chemical etching using a selective solution of succinic acid and hydrogen peroxide followed by a Ti/Pt/Au/Ti Schottky gate metal deposition. To fabricate the second 100 nm gate, we turn

a)Electronic mail: nicolas.wichmann@iemn.univ-lille1.fr.

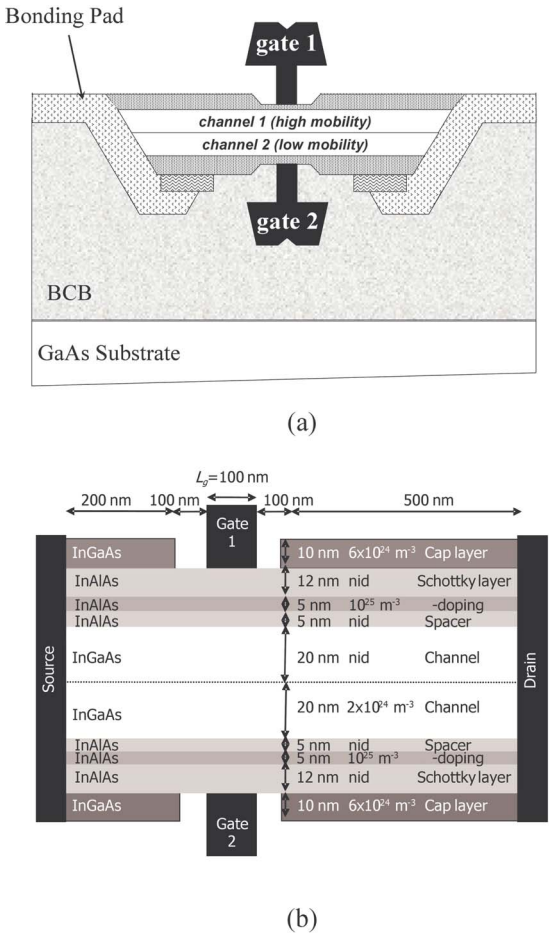

FIG. 1. (Color online) (a) Schematic cross sections of the 100 nm T-gate VMT. (b) Schematic of the simulated VMT.

around and transfer the fabricated structure onto a GaAs host substrate by an adhesion bonding technique using BCB polymer. After that, the initial InP substrate is removed with a hydrochloric acid based solution. Then, InGaAs and InP etch-stop layers are selectively etched by phosphoric acid and hydrochloric acid based solutions, respectively. Finally, the second gate recess and Schottky gate metallization are fabricated in the same way like the first gate. Figure 1(a) shows the schematic cross section of the final structure after bonding on GaAs host substrate. In order to characterize the VMT in differential mode (application of different voltages on each gate electrode) the first gate metallization (gate 1) must overlap only one mesa sidewall, while keeping a perfect gate alignment.[3]

In order to perform the electrical characterization of our VMTs, we define the DC gate voltages by means of two terms: a common mode bias voltage $V_{G\mathrm{off}}$ that controls the level of depletion under both gates and allows adjusting the total amount of electrons in the channel N_T (and therefore the drain current level) and a differential potential $V_{G\mathrm{diff}}/2$ that modulates the population of the high and low mobility channels. As a result, the gate voltages are defined as follows: $V_{G1S}=V_{G\mathrm{off}}+V_{G\mathrm{diff}}/2, V_{G2S}=V_{G\mathrm{off}}-V_{G\mathrm{diff}}/2$.

The experimental I_D-V_{DS} output characteristics and $g_{m\mathrm{CM}}$-$V_{G\mathrm{off}}$ characteristics (both for $V_{G\mathrm{diff}}=0$ V) are plotted in Fig. 2. In common mode ($V_{G\mathrm{diff}}=0$ V), the VMT operates as a classic DG-HEMT. A large extrinsic transconductance in common mode $g_{m\mathrm{CM}}$ of 1100 mS/mm is obtained due to the high charge control efficiency attributable to the dual gate architecture. The measured differential mode characteristics I_D-$V_{G\mathrm{diff}}$ for various $V_{G\mathrm{off}}$ at $V_{\mathrm{DS}}=0.2$ V are shown in Fig. 3(a). As expected, the values taken by I_D depend on $V_{G\mathrm{diff}}$ due to the velocity modulation. When increasing $V_{G\mathrm{diff}}$ the electron density is transferred from the low-μ to the high-μ channel, thus increasing the drain current. On these characteristics, we can also observe that the device does not completely pinch off. This problem appears due to the topology of the gates which do not cover the whole channel, so that a small part of the device near the mesa sidewalls is not controlled by the gates,[10] thus allowing for a certain amount of

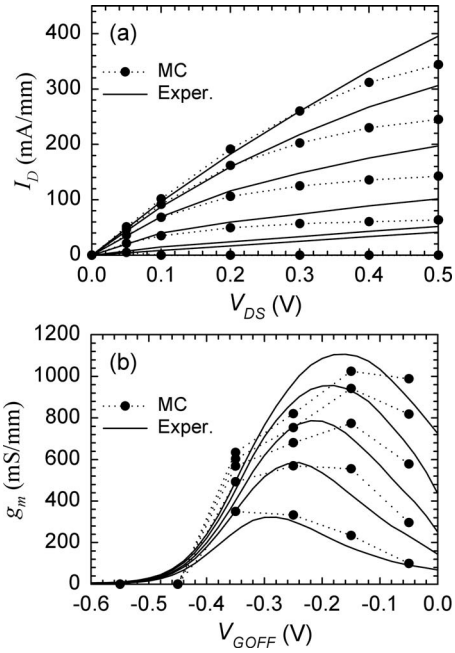

FIG. 2. Experimental and MC-simulated (a) I_D-V_{DS} curves for the 100 nm gate VMT for various $V_{G\mathrm{off}}$ at $V_{G\mathrm{diff}}=0.0$ V ($V_{G\mathrm{off}}=0$ V for the top curve and $\Delta V_{G\mathrm{off}}=-0.1$ V). (b) Common mode extrinsic transconductance $g_{m\mathrm{CM}}$ vs $V_{G\mathrm{off}}$ for different V_{DS} ($V_{\mathrm{DS}}=0.5$ V for the top curve and $\Delta V_{\mathrm{DS}}=-0.1$ V).

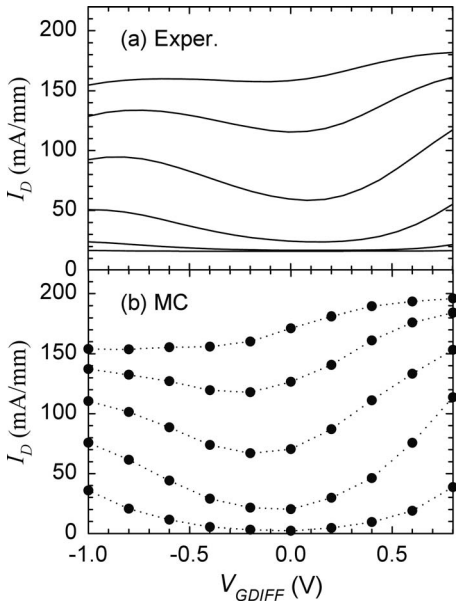

FIG. 3. (a) Experimental and (b) MC-simulated I_D vs $V_{G\mathrm{diff}}$ for $V_{\mathrm{DS}}=0.2$ V ($V_{G\mathrm{off}}=-0.1$ V for the top curve and $\Delta V_{G\mathrm{off}}=-0.1$ V).

drain leakage current. Moreover, the maximum value of the transconductance in differential mode $g_{m\mathrm{DM}}$ is about 130 mS/mm. This weak value of transconductance compared with $g_{m\mathrm{CM}}$ is directly correlated with the channel mobility ratio. This ratio must be increased to obtain high microwave performances.

In order to confirm the velocity modulation effect, the mean electron population and velocity in the two channels must be analyzed, which, as mentioned before, cannot be experimentally retrieved. With this purpose, we make use of a semiclassical ensemble MC simulator self-consistently coupled with a 2D Poisson solver accurately calibrated to correctly reproduce the static and dynamic behavior of DG HEMTs.[4,5] Our model takes into account important physical effects such as the influence of degeneracy in the channel by using the rejection technique.[8] The scheme of the simulated VMT structure, very similar to the fabricated one, is plotted in Fig. 1(b) (for simplicity, it has a symmetrical δ-doping and spacer layer). The low-μ-channel is considered to have an ionized impurity density of 2×10^{18} cm^{-3} (accounting for both acceptor and donor atoms), thus providing a mobility of 2700 cm^2/V s similar to the experimental value. Those impurities are taken into account for the electron scattering processes but not in the resolution of the Poisson equation since they are compensated.

The MC calculated common-mode I_D-V_{DS} (for $V_{G\mathrm{diff}}=0$ V) characteristics are plotted in Fig. 2(a). To compare them with the measured results, the parasitic elements, not considered in the intrinsic MC model, have been included in a postprocessing stage. Thus, the drain (R_D) and source (R_S) contact resistances have been incorporated into the original MC results, the best fit being obtained for $R_D=0.27$ Ω mm and $R_S=0.35$ Ω mm. The agreement is satisfactory at least up to $V_{\mathrm{DS}}=0.3$ V. In Fig. 3(b), the MC-simulated I_D-$V_{G\mathrm{diff}}$ curves for different $V_{G\mathrm{off}}$ at $V_{\mathrm{DS}}=0.2$ V are shown. The qualitative agreement between the experimental and MC characteristics is very satisfactory, which validates the MC model for the interpretation of the VMT microscopic performance. The increase in I_D for high negative values of $V_{G\mathrm{diff}}$ (especially for low $V_{G\mathrm{off}}$) is due to a change in N_T, associated to the nonlinearity of the dependence of the individual channel populations on V_{GS}. We will focus the analysis on the range of low $V_{G\mathrm{diff}}$ (<0.3 V), where the velocity modulation of I_D (N_T constant) is clear.

Figure 4 presents the MC results of (a) the mean number of electrons in the high-μ channel N_1, the low-μ channel N_2, the total channel N_T, and (b) the mean electron velocity in both channels as a function of $V_{G\mathrm{diff}}$ for $V_{\mathrm{DS}}=0.2$ V and $V_{G\mathrm{off}}=-0.2$ V. These values have been calculated in the region of the channel below the gate contacts. As shown in Fig. 4(a), when $V_{G\mathrm{diff}}$ is raised, N_1 increases and N_2 decreases both linearly and in the same amount, keeping constant the number of carriers. Figure 4(b) confirms the different mean electron velocity in both channels. Then, the behavior of I_D in differential mode observed in Fig. 2 for small values of $V_{G\mathrm{diff}}$ is related exclusively to the difference in the electron velocity. In other words, the variation in I_D is actually due to velocity modulation operation in the fabricated device. The next steps of this work will be to extract the dynamic parameters of our VMT by using dual-source four-port vector network analyzer and to analyze them by means of Monte Carlo simulations.

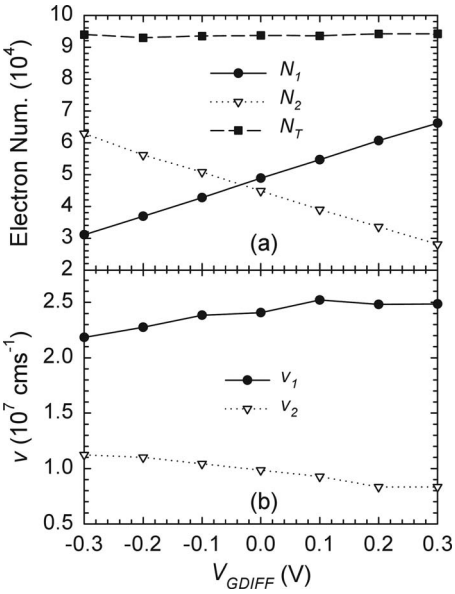

FIG. 4. MC extracted (a) number of electrons under the gate and in the high-μ and low-μ channels N_T, N_1, and N_2, respectively, and (b) mean electron velocity in the high-μ and low-μ channels v_1 and v_2, respectively, all of them as a function of $V_{G\mathrm{diff}}V_{\mathrm{DS}}=0.2$ V and $V_{G\mathrm{off}}=-0.2$ V.

In this work, we have fabricated and characterized an InAlAs/InGaAs 100 nm gate VMT. Taking as a base the fabrication process of the DG-HEMT, two gates are placed in both sides of the device to control the total charge density in the channel. The optimization of the growth conditions of the epitaxial layer allows creating two distinct channels with significantly different mobilities, which is fundamental for high charge control efficiency and to obtain a huge I_D velocity modulation effect. The good agreement between the experimental characteristics and the results of the simulations validates the MC model and demonstrates the velocity-modulation behavior of the fabricated device.

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