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Harmonic distortion in laterally asymmetric channel metal-oxide-semiconductor field-effect transistors operating in the linear regime

Raúl Rengel*,† and María J. Martín

Department of Applied Physics, University of Salamanca, Salamanca, Spain

ABSTRACT

A Monte Carlo investigation of the linear regime harmonic distortion in laterally asymmetric channel (LAC) and conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) for radio frequency applications is presented. Simulations of nonlinearities are carried out both considering the Fourier analysis in AC conditions (at 5 and 20 GHz) and the integral function method. The results show a general good agreement between both modeling techniques, with the exception of the third harmonic distortion at the higher frequency, which is underestimated by the integral function method at low gate bias. A general improvement in the total harmonic distortion and second harmonic distortion is evidenced in LAC MOSFETs as compared to conventional devices. While the third harmonic distortion at low gate bias is slightly degraded in LAC transistors, at high V_{GS}, the LAC MOSFET also improves this figure of merit as compared to conventional transistors, which confirms the suitability of LACs also for large-signal radio frequency applications. Copyright © 2013 John Wiley & Sons, Ltd.

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KEY WORDS: laterally asymmetric channel; RF MOSFET; harmonic distortion; linear regime; Monte Carlo method

1. INTRODUCTION

The study of the harmonic distortion in new generations of metal-oxide-semiconductor (MOS) transistors is critical in order to determine their suitability for radio frequency (RF) analog applications. In many cases, MOS field-effect transistors (MOSFETs) are required to operate as linear resistors in RF designs, as, for example, in integrated continuous-time tunable filters [1]: the presence of nonlinearities may be therefore an important constraint, particularly when dealing with alternative topologies to conventional silicon devices. Among the different possibilities presented in the literature, the use of channel doping engineering has been demonstrated to be a very interesting possibility in order to improve the small-signal RF performance of MOS devices. In the case of graded channel devices (which are characterized for having two different homogeneous doping regions in the channel [2]), the harmonic distortion has been extensively analyzed [1, 3]. A different alternative is the consideration of laterally asymmetric channel (LAC) MOSFETs, in which the channel doping varies gradually from source to drain [4]. This kind of devices has been proved to outperform conventional MOSFET from the static, dynamic, and high-frequency noise [4–6] point of view. However, the investigation of their harmonic distortion is a must in order to fully confirm their suitability for replacing conventional devices in RF analog designs.

In this work, we have carried out a comparative research of the harmonic distortion in LAC and conventional silicon MOSFET operating in the linear regime by means of an ensemble 2D Monte

*Correspondence to: Raúl Rengel, Department of Applied Physics, University of Salamanca, Salamanca, Spain.
†E-mail: raulr@usal.es

Carlo simulator. The analysis of the harmonic distortion is carried out using two different methods: through the Fourier analysis of AC simulations and by the integral function method (IFM) [7]. The IFM is basically a DC method, and consequently, is expected to be accurate under quasi-static conditions. However, it is extraordinarily efficient from the computational point of view as compared to AC simulations. The analysis carried out in this work allows exploring the limitations of the IFM (applied to a LAC MOSFET device) in the frequency range beyond quasi-static frequencies of operation.

The paper is organized as follows. In Section 2, the main details of the simulated structure and the simulation methodology are presented. In Section 3, the results are shown and exhaustively discussed. In Section 4, the most relevant conclusions are reported.

2. DEVICES UNDER TEST AND MODELING PROCEDURE

2.1. Devices under test

Two different structures were considered for the devices under test. The first one (Figure 1) was a LAC transistor, with a gradually varying doping profile ranging from $5 \cdot 10^{-18}\,\mathrm{cm}^{-3}$ at the source end of the channel to $10^{-16}\,\mathrm{cm}^{-3}$ at the drain end, with a realistic Gaussian profile computed by 2D ISE-DESSIS. This doping profile was subsequently considered in our Monte Carlo simulator. The LAC MOSFETs can be fabricated using a process flow similar to that of conventional MOSFETs but considering a tilted angle implantation from the source side for the threshold adjust implant after the formation of the gate electrode [5]. The second structure simulated was a conventional bulk MOS transistor with a homogeneous doping profile (symmetrical [SYM] structure) equal to $1.5 \cdot 10^{-18}\,\mathrm{cm}^{-3}$, chosen in order to keep the same threshold voltage as in the LAC MOSFET. The oxide thickness is equal to 1.8 nm, while the total gate length is 130 nm, with an effective gate length L_{eff} of 100 nm (i.e., the overlap length L_{ov} is 15 nm). The depth of the source and drain regions is equal to 30 nm. The static and small-signal RF performance of these devices was exhaustively studied in a previous work [4], as well as their high-frequency noise performance [8].

2.2. Modeling procedure

The results were obtained by means of our in-house 2D Monte Carlo simulator, which has been extensively calibrated with experimental measurements in several different types of MOSFETs [9, 10] and also in other silicon devices [11]. The simulator is self-consistently coupled to a Poisson solver and includes impurity, optical phonon, acoustic phonon, and surface scattering. In this context, because of the particular features of the Monte Carlo method applied to the simulation of semiconductor devices, a MOSFET model is not needed to obtain the *I–V* curves because they are provided by the device numerical simulation. This modeling technique is usually recognized as one of the most reliable simulation procedures, allowing performing computer experiments [12], with the only constraint of very large CPU times. More details about our simulator can be found in [4, 8–11, 13].

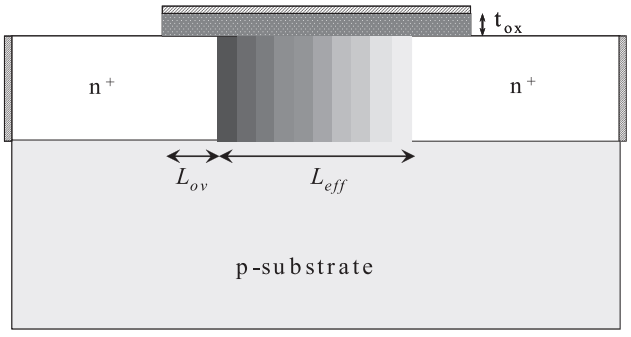

Figure 1. Scheme of the devices under test. In the case of conventional (SYM) devices, the doping in the channel is homogeneous.

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The study is focused on the linear regime, that is, considering a fixed V_{GS} and a large signal periodic variation in V_{DS}, as shown in Figure 2. As previously stated, in order to analyze the harmonic distortion both in LAC and SYM MOSFETs, two different approaches were followed. First, we carried out long-time AC simulations (at least 300 ps long), with a sinusoidal variation of the voltage applied at terminals, with a linear frequency equal to 5 and 20 GHz. The instantaneous current values are averaged over several cycles (more than six) in order to minimize the influence of numerical noise in the results. Subsequently, Fourier analysis is carried out in order to obtain the Fourier coefficients that allow determining the harmonic distortion according to [14]. As an example, Figure 3 shows

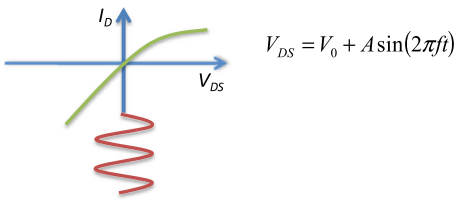

Figure 2. Schematic representation of the linear regime analysis carried out in this work. Considering a fixed V_{GS}, V_{DS} is varied according to the expression shown, A being the signal amplitude, f its frequency, and V_0 the drain current bias (0.0 V in this case).

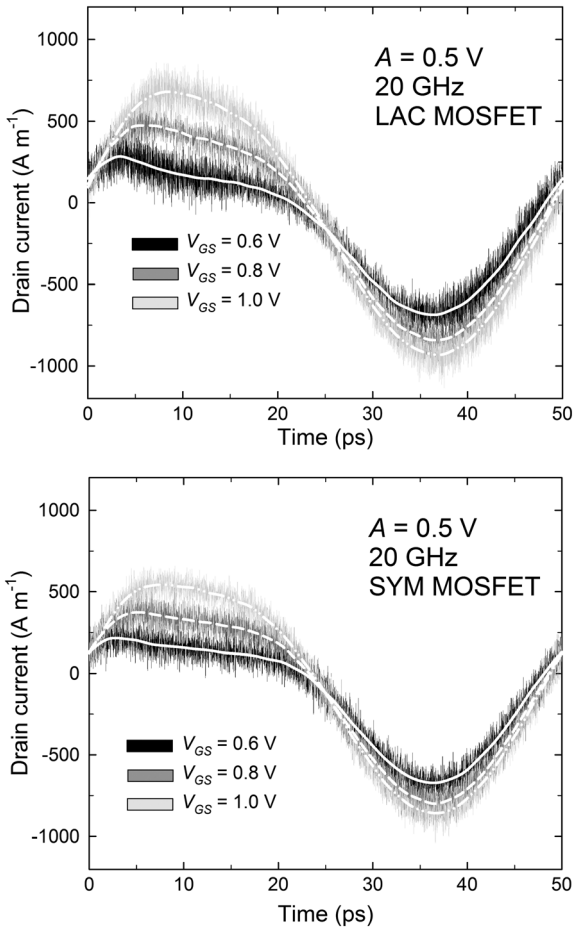

Figure 3. The AC output current for several V_{GS} values (0.6, 0.8, and 1.0 V) and a varying drain voltage $V_{DS} = V_0 + A \cdot \sin(2\pi ft)$, with $f = 20$ GHz, $A = 0.5$ V, $V_0 = 0$ V for the laterally asymmetric channel (up) and SYM (down) metal-oxide-semiconductor field-effect transistors. The white lines represent the filtered values of the current in order to provide a clearer view (solid line, $V_{GS} = 0.6$; short dashed line, $V_{GS} = 0.8$; and dash-dot-dot line, $V_{GS} = 1.0$ V).

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the results obtained for several different values of the gate voltage when a sinusoidal voltage of amplitude 0.5 V is applied to the drain.

The second technique employed in this work to calculate the harmonic distortion is the IFM [7]. This method has shown to provide very good results as compared to other techniques such as the calculation of Fourier coefficients from high order derivatives of *I–V* DC curves [15] or the use of large network spectrum analyzers to extract the distortion figures of merit from AC measurements [16]. In the IFM method, the most relevant figures of merit related to harmonic distortion can be calculated from the study of nonlinearities of DC characteristics through the calculation of a series of functions related to integral equations of *I–V* curves. In Figure 4, we present the I_D–V_{DS} curves obtained with the Monte Carlo simulator for several values of the gate voltage. From these curves, it is possible to obtain the main harmonic distortion parameters: the total harmonic distortion (*THD*), the *THD* including the DC component of the output signal (*THD0*), the second harmonic distortion (*HD2*), and the third harmonic distortion (*HD3*) as indicated in [7].

In this way, we can provide a comparison of harmonic distortion between a full AC simulation approach that includes in a natural fashion the non-quasi-static effects appearing at RF and microwave frequencies, and a DC-based method, the IFM, which is computationally more efficient.

3. RESULTS AND DISCUSSION

The Fourier coefficients (C_n) for the fundamental frequency and the second to fifth tones obtained by considering the discrete Fourier transform of the current provided in AC simulations are shown in Figure 5 for the LAC and SYM MOSFETs. Important differences can be observed for each coefficient

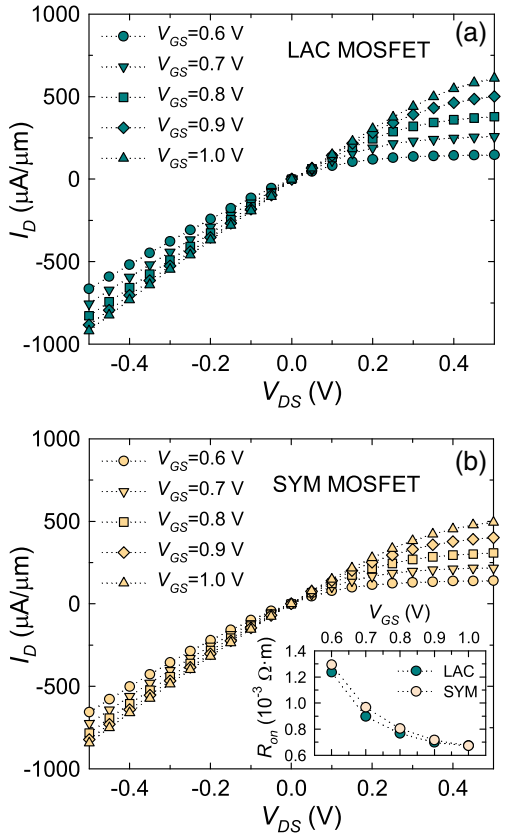

Figure 4. Output curves *I–V* for the laterally asymmetric channel metal-oxide-semiconductor field-effect transistor (a) and the conventional metal-oxide-semiconductor field-effect transistor (b) for several values of V_{GS} (from 0.6 to 1.0 V). The inset shows the values of the *on* resistance R_{on} (calculated for low V_{DS} equal to 100 mV) as a function of the gate voltage.

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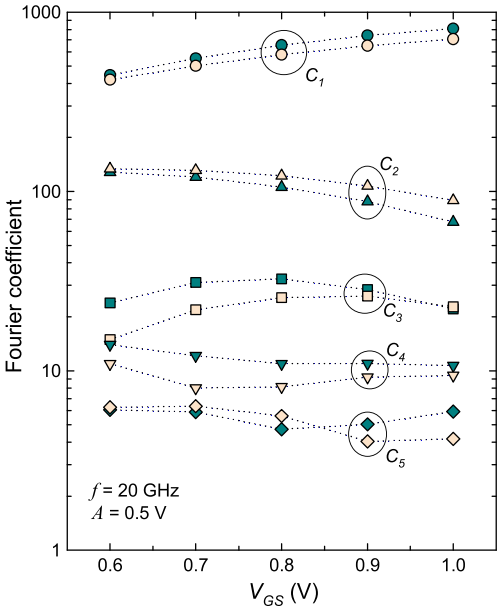

Figure 5. Fourier coefficients from C_1 to C_5 for the laterally asymmetric channel (dark symbols) and conventional (light symbols) metal-oxide-semiconductor field-effect transistors, as a function of V_{GS} for an applied signal with frequency 20 GHz, amplitude A equal to 0.5 V, and drain current V_{DS} equal to 0 V.

in both transistors. The amplitude of the fundamental frequency tends to increase with the gate bias, as it is expected, because for low V_{GS}, the triode region is reduced as compared to the case of large V_{GS}. The second harmonic tends to decrease with V_{GS}, presenting larger values in the conventional (SYM) transistor, particularly at medium and high gate voltage. However, the third and fourth harmonics have larger amplitudes in the case of the LAC transistor, which tend to reduce at large gate DC bias.

Focusing on the fundamental frequency, Figure 6 shows C_1 as a function of the input signal amplitude, and for several values of the gate voltage, from 0.6 to 1.0 V. In all cases, the LAC MOSFET provides larger output amplitude values; the difference with the SYM device increases as the signal

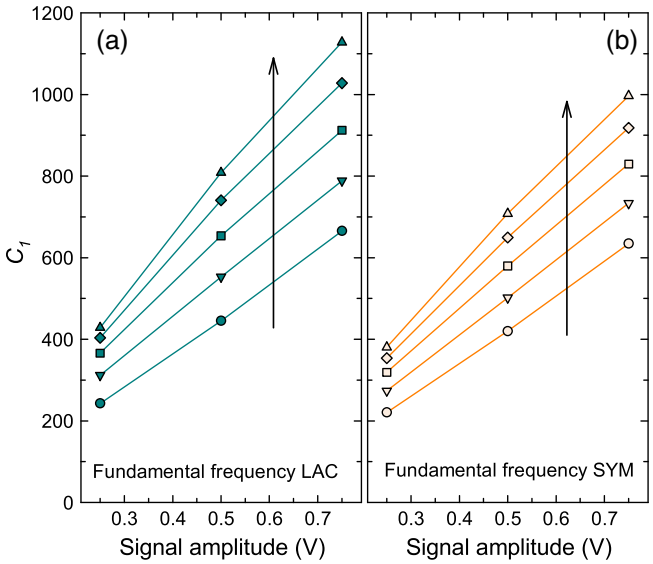

Figure 6. The C_1 coefficient for the fundamental frequency, obtained by Fourier analysis of the output AC signal, as a function of the signal amplitude for several values of the gate voltage, from 0.6 to 1.0 V (step 0.1 V), indicated by the arrows. Dark symbols correspond to the laterally asymmetric channel metal-oxide-semiconductor field-effect transistor and light symbols to the SYM.

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amplitude is larger. This is directly related to a reduced *on* resistance in the LAC MOSFETs in the linear regime (see inset of Figure 4(b)), evidenced also by the more abrupt slope in the I_D–V_{DS} curves in the case of the asymmetrically doped transistor (Figure 4), particularly at high gate bias. The reduced *on* resistance is attributed to a larger drift electric field in the channel of LAC MOSFETs observed in saturation [4], but also in the triode regime, which produces an enhanced velocity in most part of the channel as compared to a traditional transistor. In both devices, C_1 shows a practically linear dependence with the input signal amplitude.

In order to provide a more detailed analysis of the harmonic response, it is convenient to examine the distortion parameters previously mentioned in Section 2. Figure 7 shows the results provided by both the Fourier analysis of AC simulations (with an applied signal with frequency 20 GHz) and also the results obtained by the DC-based IFM, for a sinusoidal signal of amplitude 0.5 V applied to the drain contact and several values of V_{GS}. As it can be observed, the agreement between both calculations is very good for *THD0*, *THD*, and *HD2* in the whole bias range. For *HD3*, there is a good agreement for medium and high gate voltages. However, at low V_{GS}, there is an underestimation of this parameter by the IFM, which is more evident for the conventional (SYM) MOSFET. Nevertheless, at lower signal amplitudes (e.g., 0.25 V, not shown in the graphs), the agreement for *HD3* between both methods is very good and is comparable to the other distortion figures of merit, which suggests that IFM would be accurate only for not very large amplitudes.

The differences observed in Figure 7 are also related to non-quasi-static effects, which are not properly reproduced by the IFM method. At high frequencies, these phenomena (which directly affect the transconductance because of the delay time of carriers when V_{GS} is rapidly varied) can be particularly relevant for the modeling of the nonlinear behavior [17]. The AC simulation carried out by means of the Monte Carlo model properly reproduces such effects, thus providing more accurate results that the IFM, which is essentially a DC model. If a lower frequency (in the quasi-static range for these transistors, which reaches up to a few GHz, i.e., less than 10 GHz) is considered, the agreement between the IFM and the direct Fourier analysis is excellent, even for *HD3* and at low gate voltage. Figure 8 shows the results obtained from the AC simulation for *HD3* at 20 and 5 GHz. As it can be observed, the discrepancies between the AC simulations and the IFM regarding the *HD3* previously observed in Figure 7 practically disappear at 5 GHz. Therefore, the IFM method can be

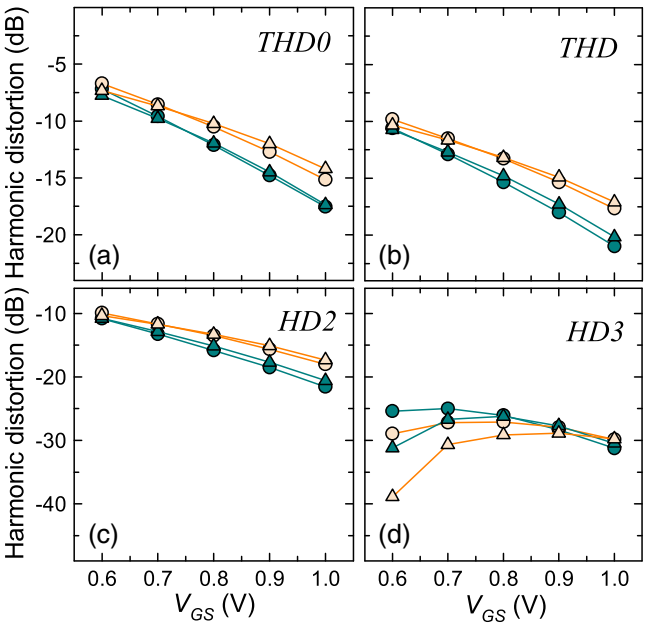

Figure 7. Comparison for the values of *THD* including the drain current component of the output signal (a), total harmonic distortion (b), second harmonic distortion (c), and third harmonic distortion (d) for the laterally asymmetric channel (dark symbols) and SYM (light symbols) metal-oxide-semiconductor field-effect transistors. Circles correspond to the values obtained through the Fourier transform of AC simulations, while triangles correspond to the values obtained using the integral function method for several values of V_{GS} and $A = 0.5$ V.

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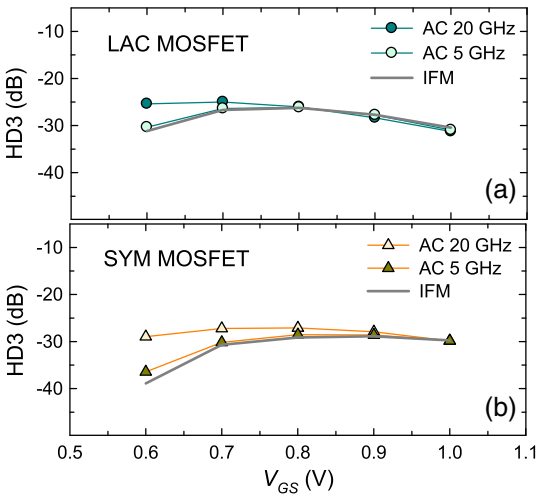

Figure 8. Values of third harmonic distortion for the laterally asymmetric channel (a) and SYM (b) metal-oxide-semiconductor field-effect transistors obtained from the integral function method (solid line) and AC analysis for a frequency equal to 20 (black symbols) and 5 GHz (white symbols).

regarded as an excellent estimator for the harmonic distortion of the devices in the quasi-static range, a conclusion which is in good agreement with the results observed by other authors [18]. If performing a frequency dependent analysis, the discrepancies observed for *HD3* could be an early indicator of a relevant influence of non-quasi-static effects.

If we focus on the differences between LAC and SYM MOSFETs, as it can be observed, better values are obtained for the LAC MOSFET for *THD0*, *THD*, and *HD2*. The differences are increased as the gate bias is increased (i.e., for higher drain currents). This indicates an improved performance of the LAC MOSFET for practical amplifier configurations and reinforces the general enhanced performance of the devices for analog RF configurations previously confirmed when dealing with the small-signal RF and noise performance [4, 8]. However, if we pay attention to *HD3* (Figure 7(d)), the situation is the opposite: the SYM MOSFET presents a better performance in this case than the LAC MOSFET. This worse performance in terms of the *HD3* evidences a slightly degraded behavior of these devices (at low and medium currents) in balanced or fully differential implementations, in which the *THD* is dominated by this harmonic [19, 20]. Within our modeling framework, it is not straightforward to provide a direct explanation for this reduced performance of the LAC MOSFET in terms of *HD3*. However, we have observed that, in the case of the LAC MOSFET, a larger drift velocity is obtained at the expense of a much elevated longitudinal electric field in the first part of the channel (because of the gradual doping profile) as compared to the conventional transistor. This implies a lower effective mobility for the LAC transistor at low V_{GS}, which could explain its worse performance in terms of *HD3*. This result is in good agreement with that observed by other authors, who have also pointed out towards mobility degradation effects as one of the major sources of *HD3* in triode configurations [20, 21].

Figure 9 shows the *HD2* and *HD3* (obtained by means of the IFM method) as a function of the input power (expressed in dBm) considering a 50 Ω generator for two different values of the DC gate voltage, 0.6 and 1.0 V. Although the IFM is not completely accurate at low gate bias and high frequencies, as seen in Figure 7, it can provide an adequate picture of the differences between the LAC and SYM devices for frequencies up to 5 GHz, being much more computationally efficient than the CPU costly fully AC simulations.

At low gate bias, the *HD2* is quite similar between both transistors, while the *HD3* is reduced for the SYM transistor, presenting a dip at approximately 6 dBm of the input power (corresponding to an AC V_{DS} signal with amplitude $A = 0.6$ V). This kind of dip in the third harmonic has been also observed in other types of devices and indicates a maximum in the input power intercept point [22]. However, at high gate bias (Figure 9(b)), *HD2* is generally significantly improved in the LAC MOSFET (with the only exception of very low input power), while *HD3* shows a better behavior in most of the input power range studied (only for input power over 5 dBm, it would provide worse

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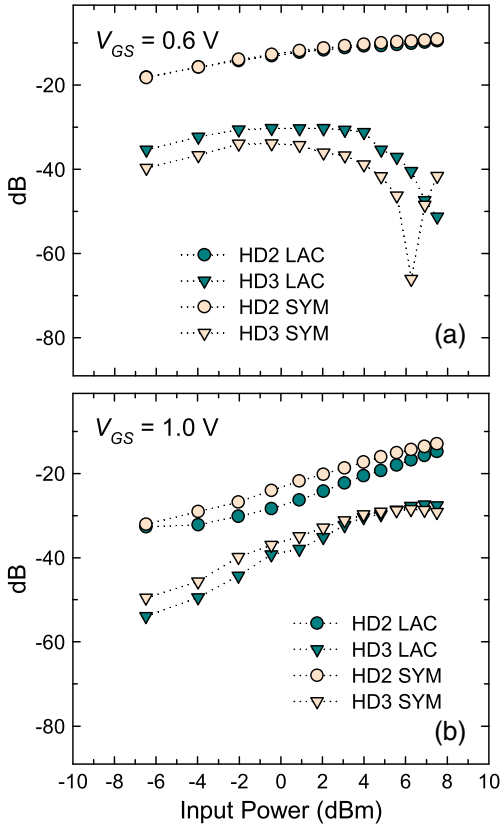

Figure 9. Second and third harmonic distortion as a function of the input power for two different values of the gate bias, 0.6 (a) and 1.0 V (b).

values of this figure of merit in the LAC device). Therefore, it can be concluded that at low gate bias, the SYM MOSFET presents a slightly better performance in terms of the *HD3*; while at high gate bias, it is the LAC MOSFET, which outperforms the conventional transistor for most of the signal amplitudes considered.

4. CONCLUSIONS

The harmonic distortion under linear regime in LAC and conventional MOSFETs for RF applications has been analyzed by means of an ensemble Monte Carlo simulator. In general, a good agreement is found between the direct Fourier analysis and the IFM for the main harmonic distortion figures of merit, with the only exception of the *HD3* at low V_{GS} and medium and high signal amplitudes, for which non-quasi-static effects play a significant role in the tens of GHz range. However, at lower frequencies (5 GHz), both methods show an excellent agreement, confirming the suitability of the IFM for the study of the harmonic distortion of asymmetric channel MOSFETs in the quasi-static frequency range.

The results obtained indicate a better amplification of the fundamental frequency in LAC devices, together with reduced amplitude of the second harmonic frequency. Regarding the *THD* and *HD2*, the LAC MOSFET features better values than symmetric channel devices, particularly at high V_{GS} (corresponding to a reduced triode resistance), thus being more adequate than conventional transistors for most analog applications. However, in the case of the *HD3* (which is particularly relevant for balanced of fully differential implementations), the gate bias considered plays a key role: at low V_{GS}, the LAC MOSFET shows a worse behavior; while at high V_{GS}, the asymmetric channel transistor generally outperforms the conventional device also in terms of this figure of merit.

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AUTHOR'S BIOGRAPHIES

Raúl Rengel was born in Tarrasa, Spain, in 1974. He received his BS and PhD degrees in physics from the University of Salamanca in 1997 and 2003, respectively. From 1998 to 2000, he was with the Electronics Group of the University of Salamanca, Department of Applied Physics, as a Grant Holder. In 2001, he became an Assistant Professor. In 2004, he was a postdoctoral researcher at the Institute d'Electronique, de Microélectronique et de Nanotechnologies, Villeneuve d'Ascq, France. He became an Associate Professor of the University of Salamanca in 2007. His main research activity is the Monte Carlo modeling of electron transport in silicon devices (including the investigation of electronic noise processes and small-signal behavior in the high frequency range in silicon on insulator metal-oxide-semiconductor field-effect transistors and non-conventional silicon devices) together with the development of simulators for the study of graphene and other 2D alternative materials.

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María Jesús Martín was born in Salamanca, Spain, in 1969. She received her BS and PhD degrees in physics from the University of Salamanca, Spain, in 1992 and 1996, respectively. Since 1992, she has been working with the Electronics Group, Department of Applied Physics of the University of Salamanca as a Grant Holder. Her graduate work focused on the simulation of transport and electronic noise in bipolar Si and SiGe structures. In 1995, she became an Assistant Professor. She worked in 1997 and in 1998 at the Electronic Components Technology and Materials of the Technological University of Delft, Delft, The Netherlands. In 2002, she became an Associate Professor of the University of Salamanca. Her current research interest is in the field of Monte Carlo modeling of electronic transport, dynamic characterization, and noise in the radio frequency range of submicrometer silicon devices, with particular focus in scaling issues and the performance of non-conventional metal-oxide-semiconductor field-effect transistors.

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