Hysteresis phenomena in nanoscale rectifying diodes: A Monte Carlo interpretation in terms of surface effects

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Hysteresis effects taking place in the rectifying current-voltage characteristic of self-switching diodes are studied by means of a semiclassical Monte Carlo simulator. When the applied voltage is higher than a certain threshold, in both negative and positive voltage sweeps, a well-defined hysteresis loop appears which can be exploited for memory applications. An algorithm for the simulation of surface effects has been introduced in the Monte Carlo simulator to explain this behavior in terms of the charging and discharging of the surface states on the etched sidewalls of the structure. Devices with different geometries have been simulated, and a detailed microscopic analysis of the behavior of surface charge and potential profiles has been performed. The reduction of the channel length or the increase of the width improves the discrimination of the memory state (by providing a higher reverse current); however, this induces a decrease of the reverse voltage threshold. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2768638]

The surface-to-volume ratio of nanoelectronic devices increases as the geometries are scaled down, so that the device behavior is more and more affected by the physical properties of the surfaces. Usually, sidewall surface states cause undesirable effects on electron transport and may drastically influence the device output characteristics. For this reason, surface or interface traps in a nanostructure are considered as a problem to avoid or eradicate. Nonetheless, in some cases these surface states may become very useful for practical applications.[1–4] This is the case of the self-switching memory (SSM) device recently proposed by Song *et al.*[1] It consists essentially of a narrow semiconductor channel with a broken symmetry, defined by trenches etched on a high-mobility modulation-doped heterostructure. If the applied voltage remains within a certain range, the *I-V* curve of the SSM is independent of the voltage sweep direction. However, beyond this bias range a pronounced hysteresis effect (suitable for memory applications) appears. The working principle of this memory point differs substantially from a conventional semiconductor one. The basis of operation of SSMs has been explained in terms of storage and release of charge at the sidewalls of the etched trenches. The aim of this letter is to propose a surface-charge model that, implemented in a Monte Carlo (MC) simulator, provides a microscopic interpretation of the memory effect, reproduces qualitatively the experimental results presented in Ref. 1, and allows performing a complete analysis of carrier dynamics in the device in order to optimize its performance.

For the correct modeling of these devices, a three-dimensional simulation would be necessary in order to take into account the effect of the lateral surface charges and the real topology of the structures. For simplicity we make use of a semiclassical ensemble MC simulator self-consistently coupled with a two-dimensional Poisson solver, where some assumptions, described in Refs. 5–7 are made. To account for the fixed positive charges of the whole layer structure, a net background doping N_{Db} is assigned to the channel, but impurity scattering is switched off; in this way, electron transport through the undoped channel is well described. Concerning surface effects, MC simulations are able to explain the physics of the self-switching operation in InAlAs/InGaAs-based SSDs (Ref. 2) by simply modeling the surface states through a *constant* (depending neither on the position nor on the applied potential) negative surface charge density σ placed at the interfaces. A value of the depletion width W_d about 40 nm (±10 nm) for $In_{0.7}Ga_{0.3}As$ channels[8] was obtained near equilibrium conditions, which corresponds to a surface charge density of $\sigma/q=(0.4\pm0.1)\times10^{12}$ cm^{-2} [using $N_{\mathrm{Db}}=10^{17}$ cm^{-3} (Ref. 2)]. While being adequate for thick channels, this model provides incorrect results for thin ones (with $W\leqslant 2W_d$), because charge neutrality is not ensured and unphysical high negative potentials may be obtained. To solve this problem we have recently proposed a model in which the local value of the surface charge σ is adjusted *self-consistently* with the surrounding carrier density.[9] This self-consistent surface charge model provides good qualitative and quantitative descriptions of the operation of the three-terminal ballistic junctions with different widths of the vertical branch in terms of the adaptation of the surface charge to the geometry and bias conditions.[9]

The variations of the surface states occupation are produced by electron transfer from/to the channel. As explained in Ref. 1 for the case of SSMs, this transmission of charge is modulated by the combination of tunneling and thermionic emission processes. In order to account for these phenomena, we have implemented an updated algorithm in our MC simulator which completes and improves the previous self-consistent charge model,[9] thus being able to describe the memory effects found in SSMs.

The philosophy of the model is as follows. First, the values of perpendicular electric field $E^{\perp}$ and electron density near the interface n_{int} are calculated as an average over a given number of iterations, 500 in our case. If the electric field $E^{\perp}$ exceeds a "discharging threshold value" E_{dis} and the neighboring concentration n_{int} is smaller than a "discharging level" n_{dis} (relative to the background doping),[9] the local

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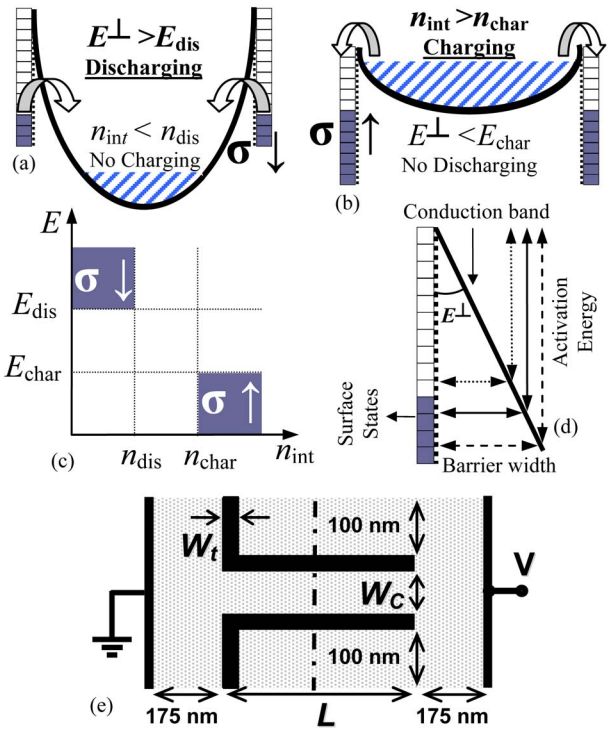

FIG. 1. (Color online) [(a) and (b)] Sketch of the conduction-band profiles in the channel along the dashed line in (e) for different bias voltages. (a) Discharging of surface states by tunneling into the channel. (b) Charging of surface states by thermionic emission from the channel. (c) Scheme of the different conditions considered in the surface charge algorithm. (d) Illustration of the relation existing among the activation energy of the surface states, the perpendicular electric field and the barrier width. (e) SSM geometry (W_c the channel width, L the channel length, and W_t the trench width).

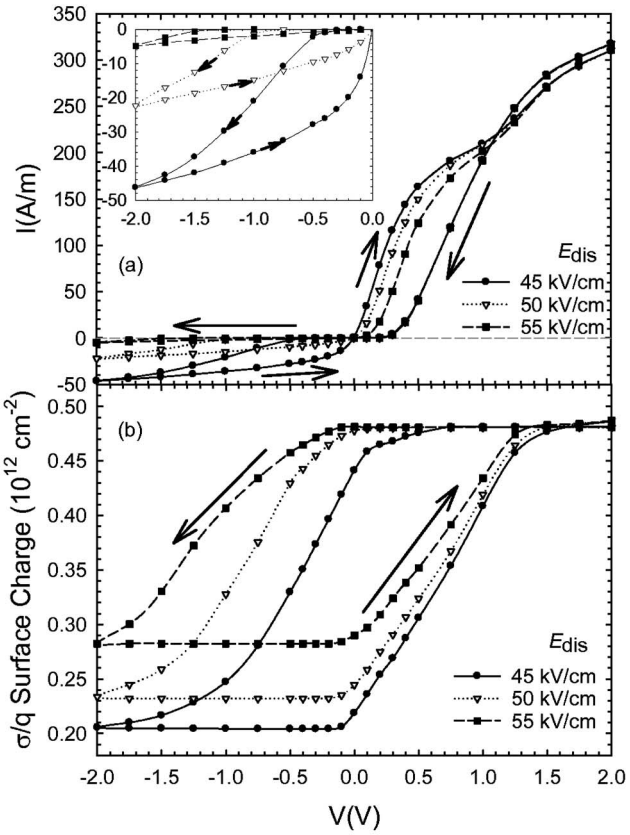

FIG. 2. (a) *I-V* curves of SSMs with different E_{dis}. The inset shows a zoom of the reverse bias loop. (b) Average value of the surface charge in the sidewalls of the channel.

value of σ is decreased in the simulation in a value $\Delta\sigma = 10^{-10}$ cm^{-2}. The field condition reflects the fact that the slope of the conduction band in the channel perpendicular to the interface is sufficiently high (the barrier is thin enough) to have large probability for tunneling processes which discharge surface states [Fig. 1(a)]. Moreover, since n_{int} is small, surface state charging processes are negligible as compared to the tunneling charge release. On the other hand, if the perpendicular electric field $E^{\perp}$ is lower than a charging threshold value E_{char} and the carrier density is higher than a charging level n_{char},[9] the dominating mechanism is the filling of surface states by thermionic emission, and σ is raised in the same quantity $\Delta\sigma$ [Fig. 1(b)]. In the cases in which the electric field and the free carrier concentration do not fulfil these conditions [situations sketched in Fig. 1(c)], charge trapping and release are considered to be negligible or approximately compensate each other and the value of σ is kept constant. The values used for the limit concentrations are $n_{char} = N_{Db}/50$ and $n_{dis} = N_{Db}/100$.

Since the electric field is the slope of the potential barrier existing between the surface states and the channel, the threshold values E_{dis} and E_{char} could be connected with the activation energy of the surface states and the barrier width, as shown in Fig. 1(d). The higher the activation energy, the higher the slope of the conduction band necessary to attain a barrier thin enough to have a significant probability of electron tunneling into the channel.

We have simulated InGaAs SSMs at 300 K with the geometry shown in Fig. 1(e) (with $W_c = 60$ nm, $L = 250$ nm, and $W_t = 10$ nm) and different discharging threshold fields E_{dis} [Fig. 2(a)] (always with $E_{char} = 20$ kV/cm). By means of the microscopic quantities provided by the MC simulator we can provide an explanation for the hysteresis effects in terms of the population of the surface states at the channel sidewalls. Figure 2(b) shows the average surface charge density at the sidewalls of the channel. A maximum value of $\sigma/q = 0.5 \times 10^{12}$ cm^{-2} is allowed, corresponding to a total occupation of the surface states. The voltage sweep starts from 2 V, when the surface states are fully occupied, and then follows the direction of the arrows. When decreasing V down to 0.0 V, the current takes the same values for the different E_{dis} because the surface charge remains essentially constant, as observed in Fig. 2(b). When going to negative voltages, the sidewall surface charge significantly decreases, thus allowing the current flow (let us remind that for values lower than $\sigma/q \approx 3 \times 10^{15}$ m^{-2}, for which $W_d \approx W_c/2$, the channel is open). The higher the value of the discharging field, the higher the negative threshold voltage necessary to release the surface charge and allow the current flow. Additionally, the reverse current level also decreases for higher E_{dis} due to the larger amount of surface charge remaining in the surface states for a given applied voltage [Fig. 2(b)].

When sweeping the voltage upward from $V = -2.0$ V, the surface charge does not change until a significant number of electrons fill the channel and $n_{int} > n_{char}$, situation that is only reached when a positive bias is applied. In contrast with the downward sweep, the direct current now is different for each E_{dis}, since, even if the evolution with V is similar, the initial value of the surface charge is not the same. An interesting feature appears at around $V = +1$ V, where the upward and downward *I-V* curves exhibit a crossover, also found in the

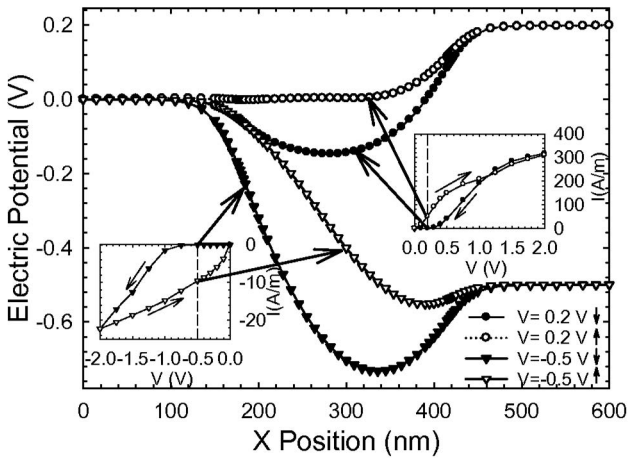

FIG. 3. Profiles of electric potential along the channel for different bias conditions. The inset shows the *I-V* characteristic in forward and reverse biases (E_{dis}=50 kV/cm).

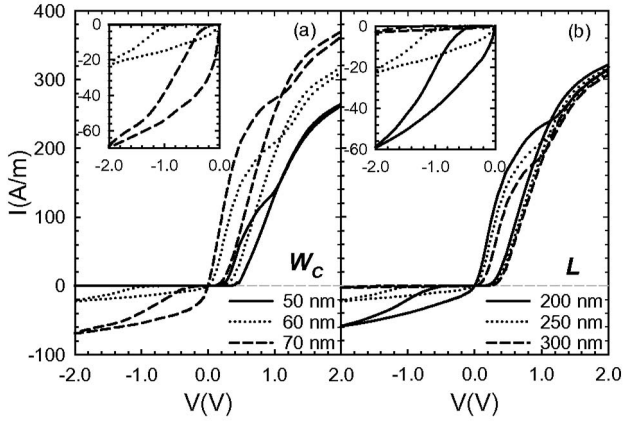

FIG. 4. Influence of the (a) width and (b) length of the channel on the *I-V* characteristic (E_{dis}=50 kV/cm).

experimental measurements.[1] As observed in Fig. 2(b), surface charges are saturated around this voltage in the downward loop, but in the upward case they are still increasing, so that the surface charge profile is still evolving. Indeed, just at $V=+1$ V there is a change in the curvature of the average surface charge in the upward loop, that reflects in a different current evolution, exhibiting a weaker increase with V and thus leading to a cross over.

From the evolution of the current with the surface charge it becomes clear that if the reverse applied voltage is not enough to empty the surface states, the device *I-V* curve will correspond to the standard rectifying behavior of a typical SSD,[2] and no hysteresis loop will be found. Such a hysteresis effect can be used for memory applications. Two different binary memory states can be clearly distinguished for both +0.2 and −0.5 V. The switch between both memory states can be performed by applying a ±2 V pulse (+2 V to set a "1" and −2 V to set a "0"), and the reading by +0.2 or −0.5 V test pulse.

In order to understand the hysteresis loop, Fig. 3 shows the electric potential along the channel inside the SSM with E_{dis}=50 kV/cm for different bias points (indicated in the inset). For V=0.2 V, if the voltage is sweeping downward from +2 V, when the surface states are almost totally filled, the potential profile shows a pronounced barrier for the electron movement in both directions (closed channel). On the contrary, when the states have not yet been charged (upward sweep), the potential barrier for the electrons moving from left to right is removed, allowing the electron flow. Similar results are found for $V=-0.5$ V; after the discharging of the surface states (arriving at −2 V and sweeping up), the right-to-left barrier practically disappears, allowing a nonzero value of the reverse current.

In order to optimize the memory operation, we have simulated SSMs where the width W_c [Fig. 4(a)] and the length L [Fig. 4(b)] of the channel are varied. The thinner the channel, the higher the negative bias needed to achieve hysteresis. Similarly, the positive threshold voltage needed to switch on the conduction is higher when the channel is narrowed. Concerning the length, current in longer channels is smaller (due to the higher impedance) and hysteresis phenomena in the reverse region are less pronounced, exhibiting a higher threshold voltage. As a general behavior, when the aspect ratio (L/W_c) is decreased, the potential barrier limiting the electron flow is smaller, so that the discharging condition of the sidewall states is reached for lower bias (soft hysteresis loop) and a significant reverse current flows.

In conclusion, by means of an improved surface charge model, based on threshold values of electric field (normal to the interface) and carrier concentration (in the vicinity of the surface) to increase/decrease the density of charge trapped in the surface states, we have provided a MC interpretation of the operating principle of SSMs. The influence of the geometry dimensions on the memory operation has been analyzed. The memory effect has been related to the thresholdlike voltage dependence of the sidewall surface charge controlling the conductance of the channel.

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