



Monte Carlo simulation of electronic characteristics in short channel δ -doped AlInAs/GaInAs HEMTs

Javier Mateos^a, Tomás González^{a,*}, Daniel Pardo^a, Virginie Hoel^b,
Alain Cappy^b

^a *Departamento de Física Aplicada, Universidad de Salamanca, Plaza de la Merced s/n, 37008 Salamanca, Spain*

^b *Institut d'Electronique et Microélectronique du Nord U.M.R. C.N.R.S. No. 9929, Département Hyperfréquences et Semiconducteurs, BP 69, 59652 Villeneuve D'Ascq Cédex, France*

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Abstract

We present a microscopic analysis of electronic noise in short channel δ -doped AlInAs/GaInAs HEMTs. A classical Monte Carlo device simulation, appropriately modified to locally introduce the effects of electron degeneracy and nonequilibrium screening, is used for the calculations. Even if the energy quantization in the channel is not taken into account in the Monte Carlo model, its validity has been checked by means of the comparison with experimental results of static characteristics, small signal behavior and noise performance in a recessed 0.1 μm T-gate δ -doped HEMT (InP based). The geometry and layer structure of the simulated HEMT is completely realistic, including recessed gate and δ -doping configuration and also the T-shape of the gate and the dielectric disposition has been included in the simulation © 2001 Elsevier Science Ltd. All rights reserved.

1. Introduction

With the aim of increasing the cut-off frequency of transistors, its gate length, L_g , has been reduced to the technological limit. However, this scaling process has the drawback that the parasitic gate resistance, r_g , increases proportionally to $1/L_g$, thus deteriorating the transconductance and, consequently, other important figures of merit of the devices like current gain and noise figure. Accordingly, while decreasing L_g , the value of the parasitic gate resistance must be kept as low as possible. A good compromise between these two requirements is the use of the T-gate technology [1,2], which allows to have a short L_g (corresponding to the base of the T) with a low value of r_g , similar to that associated to a longer gate (corresponding to the head of the T). The wider is the head of the T-gate the lower is r_g , but at the same time the gate capacitance increases [2]. Therefore the width of

the T-gate head must be chosen as a trade-off between low resistance and low capacitance. The use of the recessed geometry to improve the device characteristics is also widespread. All these refinements lead to a rather complex configuration difficult to simulate. Indeed, usually Monte Carlo (MC) simulations of MESFETs and HEMTs only consider the transport and electric field inside the semiconductor. This approach is not completely correct, since it does not take into account the capacitive coupling between the semiconductor and the T-gate taking place through the dielectric (generally Si_3N_4) used to passivate the devices. In this work we will perform the simulation of the complete configuration and its validity will be checked through the comparison with experimental measurements of I - V characteristics, small signal equivalent circuit elements, and minimum noise figure of a real 0.1 μm recessed gate δ -doped HEMT.

2. Monte Carlo simulation

For the calculations we use a semiclassical ensemble MC simulator self-consistently coupled with a 2D

* Corresponding author. Tel.: +34-923-294436; fax: +34-923-294584.

E-mail address: tomasg@gugu.usal.es (T. González).

Poisson solver (finite differences scheme, LU decomposition method) which allows the resolution of the potential in complicated geometries and nonuniform meshes. Three non-parabolic spherical valleys (Γ , L and X) with ionized impurity, alloy, polar and non polar optical phonon, acoustic phonon and intervalley scattering mechanisms are taken into account. Material parameters for the $\text{Al}_{0.48}\text{In}_{0.52}\text{As}$ and $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ are reported in Ref. [3].

The devices are divided into meshes 50 Å long and 10–100 Å wide depending on the doping and the required resolution of the potential along the structure. They are simulated at 300 K during a number of time steps (1 fs each) ranging from 20 000 for the evaluation of the I – V characteristics to 200 000 for the noise calculations. Ohmic boundary conditions are considered in the source and drain contacts, which are placed vertically adjacent to different materials. Accordingly, nonuniform potential and concentration profiles are considered along these contacts: those that would be obtained if real top electrodes were simulated [3–5]. The effect of degeneracy has been introduced by using locally the classical rejection technique, where electron heating and nonequilibrium screening effects are introduced by means of the local electron temperature [3,6].

Let us focus now on the boundary conditions used for the Poisson solver, which are of great importance for the simulation of the T-gate geometry. A static charge is placed in the surface of the semiconductor in order to model the effect of its surface potential (which pins the Fermi level close to the middle of the energy gap). The value of the surface charge is taken as a parameter which allows the fitting of the experimental I – V characteristics [3,4]. The boundary condition associated with this surface charge is $D_1 - D_2 = \sigma_{12}$, D_i being the displacement vector normal to the surface of the material labeled i (that can be the semiconductor, the dielectric or the air). σ_{ij} is the surface charge associated to the interface. If there is no surface charge at the interfaces (i.e. between two different dielectric materials), the continuity of the displacement vector normal to the surface is imposed. Finally, a fixed potential is applied to the contacts (Dirichlet condition) and zero normal electric field at the limits of the simulation domain (von Neumann condition). More details about the MC simulation can be found elsewhere [3,4,7].

3. Device structure

The SEM photographs of the cross-section of a real 0.1 μm recessed-gate δ -doped HEMT fabricated at the IEMN shown in Fig. 1(a) outline the geometry of the usual recessed T-gate configuration [2,3]. The layer structure of this HEMT, which has been reproduced in the simulation, was already presented in Ref. [3] and

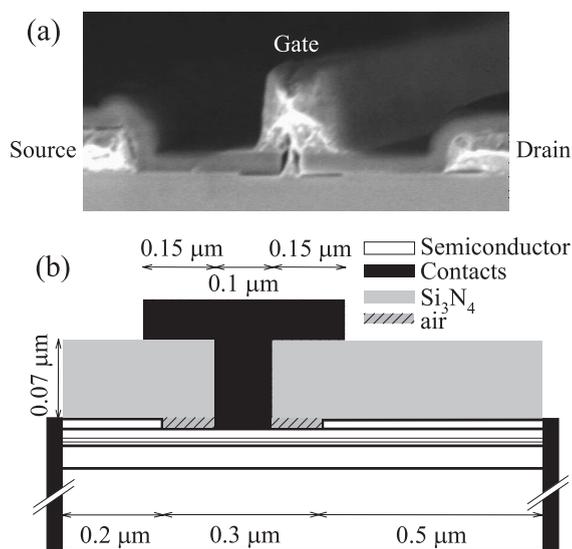


Fig. 1. SEM photograph of the cross section of a real recessed T-gate-HEMT (a) and its simplified representation used for the MC simulation (b).

consists of an InP substrate, a 3000 Å $\text{Al}_{0.48}\text{In}_{0.52}\text{As}$ buffer followed by a 250 Å thick $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ channel, three $\text{Al}_{0.48}\text{In}_{0.52}\text{As}$ layers (a 50 Å spacer, a $5 \times 10^{12} \text{ cm}^{-2}$ δ -doped layer modeled as a 50 Å layer doped at $N_D = 10^{19} \text{ cm}^{-3}$ and a 100 Å Schottky layer) and finally a 100 Å thick $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ cap layer ($N_D = 5 \times 10^{18} \text{ cm}^{-3}$). Note also the presence of two air islands inside the recess, one at each side of the gate, originating from the fabrication process, which will be also considered in the simulation. Indeed, the simulated devices, sketched in Fig. 1(b), have exactly the same layer distribution as that of the real HEMT, and almost the same geometry. The vertical position of the source and drain contacts does not introduce any significant change in the results. Contact resistances are included in a post-processing stage, where the non-simulated ohmic source region is also considered by adding an extra contribution to the resistance of the source contact [3]. The rest of features of the real HEMTs have been simulated as closely as possible.

4. Results

By adjusting separately the surface charge on the cap layer and on the bottom of the recess (whose values are, respectively, $6.2 \times 10^{12} \text{ cm}^{-2}$ and $4.3 \times 10^{12} \text{ cm}^{-2}$), the static I – V characteristics of the real HEMT have been reproduced quite closely by the simulation (Fig. 2).

In order to evidence the influence of the T-shape of the gate on the potential distribution, Fig. 3 shows the

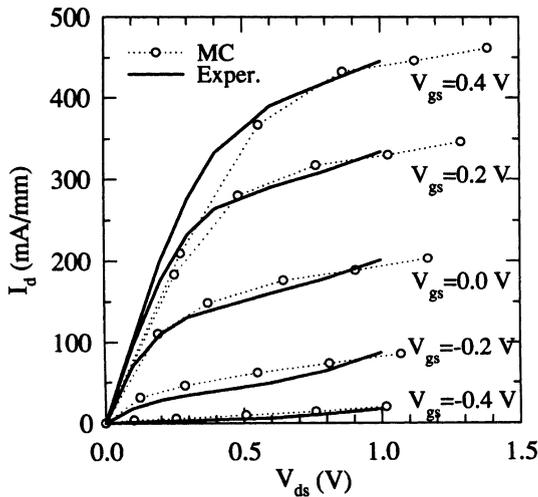


Fig. 2. Comparison of the I - V characteristics measured in a real HEMT (—) with those obtained from the MC simulation (···○···).

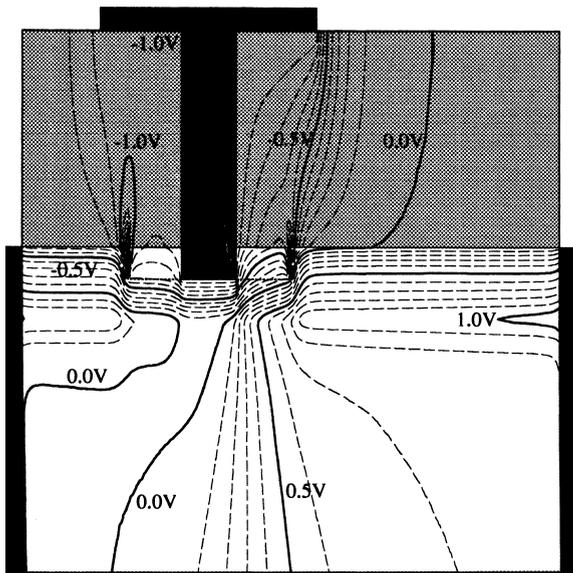


Fig. 3. Equipotential lines for an intrinsic bias of $V_{ds} = 0.75$ V, $V_{gs} = -1.0$ V.

equipotential lines calculated with the MC simulation. The intrinsic bias is $V_{ds} = 0.75$ V, $V_{gs} = -1.0$ V, corresponding, approximately, to an extrinsic bias of $V_{ds} = 0.79$ V, $V_{gs} = -1.02$ V. We can observe how the equipotential head of the T-gate influences the distribution of the potential in the dielectrics (silicon nitride and air). This influence even penetrates into the semiconductor area under the recess, leading to a horizontal enlargement of the depletion region under the gate and thus increasing slightly the effective gate length.

As next step in the characterization process, we evaluate the intrinsic small signal equivalent circuit of the transistor, taking as a base the Y parameters calculated by means of the Fourier analysis of the transient response of the transistor to voltage steps applied to the gate and drain electrodes. The modelling of the T-gate in the simulation is necessary due to the strong capacitive coupling existing between the head of the gate and the semiconductor, which affects the values of the gate-source, C_{gs} , and gate-drain, C_{gd} , capacitances.

In Fig. 4 we show the simulated and measured values of the capacitive elements of the intrinsic small signal circuit as a function of the drain current (under an extrinsic drain bias of 0.8 V). Since not all the parasitic capacitive effects have been taken into account in the simulation, the MC results have been shifted by a constant value in order to fit the experimental values at zero current (where it remains only the effect of the geometric capacitances, which are independent of the biasing). The shifting values are $+2.2 \times 10^{-10}$ F/m for C_{gs} , $+0.7 \times 10^{-10}$ F/m for C_{gd} and -0.3×10^{-10} F/m for C_{ds} (quite reasonable values considering the technology used). Once this adjustment has been made, a good agreement between experimental and simulated results is achieved.

Another important small signal parameter is the intrinsic cut-off frequency f_c , that can be calculated as $f_c = g_m/2\pi C_{gs}$ (with g_m the transconductance). In Fig. 5 we present the comparison between the experimental and the MC results for f_c , both showing a maximum of about 270 GHz and a good overall agreement.

At this point we have to recall that the precision of the MC method is not very high when calculating the

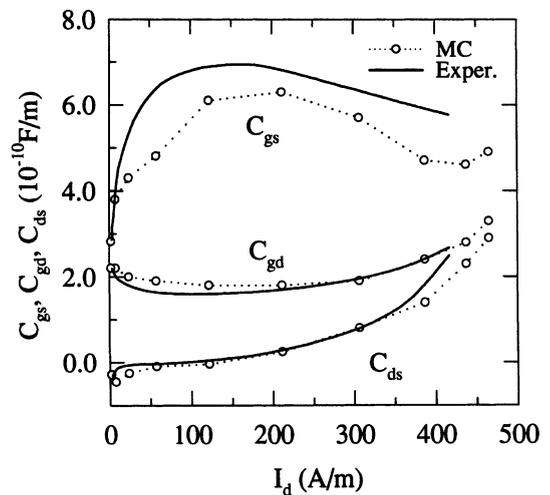


Fig. 4. Capacitive elements of the intrinsic small signal equivalent circuit, C_{gs} , C_{ds} and C_{gd} , as a function of I_d for an extrinsic bias $V_{ds} = 0.8$ V.

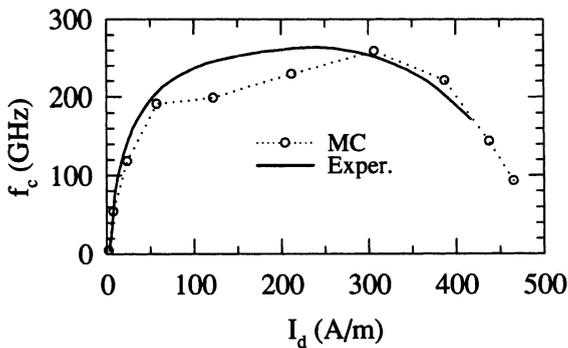


Fig. 5. Cut-off frequency $f_c = g_m/2\pi C_{gs}$ as a function of I_d for an extrinsic bias $V_{ds} = 0.8$ V.

small signal equivalent circuit elements. Actually the error can be more than 10% (20% in the case of second order parameters like f_c). That is why MC results are usually used to obtain the qualitative behavior of the different electronic characteristics, but very few attempts to reproduce experimental results have been made. In our case the values obtained for the capacitances and f_c are quite similar to the experimental data, which, taking into account the intrinsic MC uncertainty, can be considered as a very satisfactory result. Moreover, it is especially remarkable the fact that their dependence on the drain current is closely reproduced.

Once static and dynamic characteristics have been determined, we will perform the study of the noise behavior of the device. The parameter most commonly used to characterize the noise performance of real devices is the minimum noise figure, F_{min} [1,4]. It indicates the amount of noise power that an active device introduces in the signal that is amplifying. Fig. 6 shows the

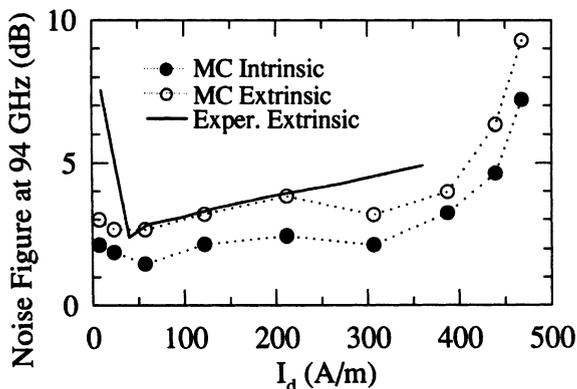


Fig. 6. Extrinsic F_{min} obtained with the MC ($\dots\circ\dots$) and experimentally (---) at 94 GHz as a function of I_d for an extrinsic bias $V_{ds} = 0.8$ V. For comparison, the intrinsic F_{min} obtained with the MC (\bullet) is also plotted.

good agreement found between experimental and simulated values of the extrinsic F_{min} , both showing a minimum of about 2.6 dB at $I_d \approx 60$ A/m. The increase of F_{min} at low current is not completely well reproduced by the simulations since it is not possible to calculate accurately the small signal parameters at low I_d , when g_m is practically null. Moreover, the uncertainty of the noise figure carries the error related to the small signal elements and also to the noise parameters, thus giving a possible deviation of more than ± 0.5 dB.

The important increase of the extrinsic with respect to the intrinsic values of F_{min} is originating from the parasitic elements, mainly the gate resistance. The aim of the T-gate technology is just the reduction of the gate resistance, r_g , and, consequently, of F_{min} . To clarify the importance of r_g , in Fig. 7 we show the extrinsic value of F_{min} (at $I_d \approx 60$ A/m where it takes the minimum value) calculated as a function of r_g at 94 GHz. It can be clearly observed how the noise of the devices increases strongly with the increase of r_g . Particularly, our T-gate HEMT has $r_g = 5.3 \Omega$, leading to an extrinsic F_{min} as low as 2.6 dB. In the case of devices fabricated without the T-gate configuration r_g is much higher (about seven times), thus increasing significantly F_{min} up to a value of nearly 6 dB. These results demonstrate the great potentiality of the T-gate technology for the fabrication of low-noise amplifiers.

We must remark that in Fig. 7 we consider that the only variable parameter is r_g , assumption which is not completely exact, since some other parameters would change when the gate is modified. Specially, C_{gs} and C_{gd} will be reduced when the T-gate configuration is not used, thus reducing F_{min} . Anyway, this effect is much smaller than the increase associated with the higher r_g . Therefore, even if Fig. 7 somewhat exaggerates the increase of F_{min} , its dependence with r_g is reasonably reported.

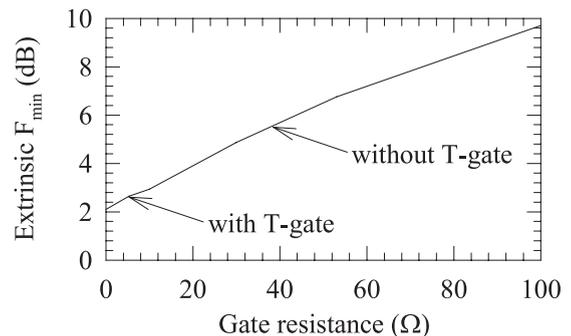


Fig. 7. Extrinsic F_{min} as a function of the gate resistance (for our T-gate HEMT $r_g = 5.3 \Omega$, without T-gate r_g is about 40 Ω).

5. Conclusions

Taking as a basis the geometry and parameters of a real structure, and using a MC simulation, we have performed a realistic analysis of a AlInAs/GaInAs, InP based HEMT, where the T-gate configuration has been included for first time in the MC simulations. The $I-V$ characteristics, small signal equivalent circuit parameters and minimum noise figure measured in a real device are favorably compared with the simulation results. We have confirmed the importance of reducing the gate resistance to diminish the noise figure of the devices. To this end the use of the T-gate technology is a very efficient method.

Acknowledgements

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