Monte Carlo Study of Dopant-Segregated Schottky Barrier SoI MOSFETs: Enhancement of the RF Performance

María J. Martín-Martinez, Carlos Couso, Elena Pascual, and Raúl Rengel

***Abstract*— This paper presents a detailed Monte Carlo study of the optimization of the dopant segregation (DS) layer in n-type Schottky barrier (SB)-MOSFET. It is shown that with a careful control of the DS layer parameters, dopant concentration (N_{dop}), and length (L_{dop}), the performance of the devices is significantly enhanced. The presence of the DS layer induces crucial effects in the injection processes at the Schottky contacts. The benefits of increasing the length and the doping level of the DS layer are studied from the microscopic point of view (transit times, average number of scatterings). The effect of varying these parameters is also analyzed through the nonquasi-static parameters of the small signal equivalent circuit, which can be useful for designers to improve the reliability of the SB-MOSFET technology.**

***Index Terms*— Dopant segregation (DS), Monte Carlo methods, RF performance, Schottky barrier (SB)-MOSFETs.**

I. Introduction

SCHOTTKY barrier (SB)-MOSFET devices present low values of the contact resistance, high scalability, and reduced short channel effects, together with a high transconductance [1], [2]. Their structure is rather similar to conventional MOSFETs, and therefore fully compatible with silicon CMOS technology [3]. The main difference relies in that the heavily doped source and drain regions in traditional MOSFETs are replaced by silicides, to form Schottky contacts: injection of charge inside the channel is due to thermionic or field emission (direct quantum tunneling) processes at the source contact [4], [5]. To obtain current levels suitable for practical applications, the use of materials providing low values for the SB is imperative. However, even using rare earth silicides (which provide the lowest known barriers for n-type silicon), it is not possible to reach the barrier height values as low as requested [6]. To tackle this issue, the introduction of a dopant segregation (DS) layer adjacent to the Schottky interface can be a prime choice [7]. This thin, highly doped layer induces a strong band bending close to the contact enhancing the tunneling probability (and consequently also the drive current), as exemplified in [6]–[13]. Several authors have disclosed the advantages of DS layers, focusing on the reduced effective barrier height, the I–V curves, the parasitic contact resistance, the ON–OFF current ratio or the variation of the threshold voltage [6], [8], [12], [14]–[23] proving that the use of DS layers provides higher performance SB-MOSFETs for several analog and digital applications. However, few studies address the effects of the presence of a DS layer on the transconductance or cutoff frequency of SB-MOSFETs [17], [19], [24], [25]. The aim of this paper is to provide an in-depth analysis of the optimization of the DS layer characteristics in an n-type SB-MOSFET by means of ensemble Monte Carlo (EMC) simulation. This analysis consists of two parts. First, a microscopic analysis focused on the study of the injection at the source contact together with internal transport quantities of interest, such as the transit times, average velocity of the carriers, number of scatterings, and so on provided by our Monte Carlo simulator. Second, a macroscopic analysis, including the drive current and the main RF figures of merit (FoM) as g_m, f_T, and power-delay-product (PDP), identifying in addition the physical processes behind the behavior of the nonquasi-static small-signal equivalent circuit (SSEC) parameters as the channel resistance or the transconductance delay time.

II. Monte Carlo Model and Simulated Device

A 2-D EMC device simulator [26], [27] has been used to obtain the results shown in this paper. It considers the most important transport processes across the Schottky interface, such as thermionic injection and absorption, together with tunneling processes (field emission and tunneling absorption), which are incorporated in the model using the Wentzel-Kramer-Brillouin approach [28], [29]. The reduction of the effective barrier [30], [31] due to the image force effect has also been carefully included [28]. The model has been calibrated with experimental data of large barrier height diodes taking the Richardson constant as the fitting parameter to provide zero current under equilibrium conditions [17]. It has provided also accurate results for fabricated back-to-back Schottky diodes [28], as well as compared with Atlas/Silvaco simulation for SB-MOSFETs [29]. The parameters of the

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M. J. Martín-Martinez, E. Pascual, and R. Rengel are with the Departamento de Física Aplicada, Universidad de Salamanca, Salamanca 37008, Spain (e-mail: mjmm@usal.es; elenapc@usal.es; raulr@usal.es).

C. Couso is with the Departament d'Enginyería Electrònica, Universitat Autònoma de Barcelona, Barcelona 08193, Spain (e-mail: carlos.couso@uab.es).

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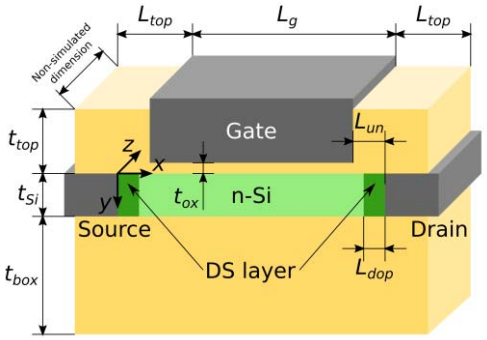

Fig. 1. Scheme of the simulated device.

SSEC circuit considered [29] are obtained from the admittance ones, given by the Fourier analysis of the transient response of the current, as shown in [32]. More details about the EMC device simulator employed can be found elsewhere [29], [33]. The number of simulated carriers is over 20 000 for all the DS layer configurations and bias conditions considered, and the timestep for self-consistently solving Poisson equation is 1 fs.

Realistic structures have been chosen for the simulated devices (gate length, L_g, equal to 120 nm and underlap length, $L_{\rm un}$, of 5 nm, see Fig. 1), quite similar to the p-type one analyzed in [17] using an Atlas/Silvaco simulator. The top oxide thickness and length, $t_{\rm top}$ and $L_{\rm top}$, respectively, are both 50 nm. The gate oxide thickness is 2.2 nm, whereas the buried oxide thickness is considered to be 400 nm. For this active layer thickness of 10 nm, the influence of quantum confinement is neglected since it is not expected to qualitatively modify the results [29]. The channel doping, $N_{\rm Dsi}$, is 10^{15} cm^{-3}. For the simulation of the DS layer, a box-shaped profile of doping $N_{\rm dop}$ and length $L_{\rm dop}$ has been considered, which represents a reasonable approximation to fabricated DS layers that rapidly fall off away from the contact electrode-channel interface [14], [16]–[18]. This box-like profile provides results quantitatively similar to considering a sharp Gaussian decaying profile, while minimizing the computer memory used in the simulations. Considering the limits of the activation of As dopants in silicon at the implantation temperatures of interest [10], [13], the values of $N_{\rm dop}$ range from 5×10^{18} cm^{-3} to 10^{20} cm^{-3}, and the DS length varies from 3 to 10 nm, which are commonly used values in experimental devices [11], [14], [17], [35]. The nominal barrier height value considered in this paper (0.28 eV) corresponds to the minimum barrier achieved in the state-of-the-art n-type contacts [6], [7], [11], [13], [15], [16], [36], and it is similar to values considered in simulations [16], [20], [22]. An SB-MOSFET device without DS has been also simulated for comparison purposes.

III. Results and Discussion

Fig. 2 shows the drain current as a function of the gate overdrive, $V_{\rm ov}$ (i.e., $V_{\rm GS} - V_T$) and $V_{\rm DS} = 2$ V for several $N_{\rm dop}$ values, with two constant $L_{\rm dop}$ values equal to

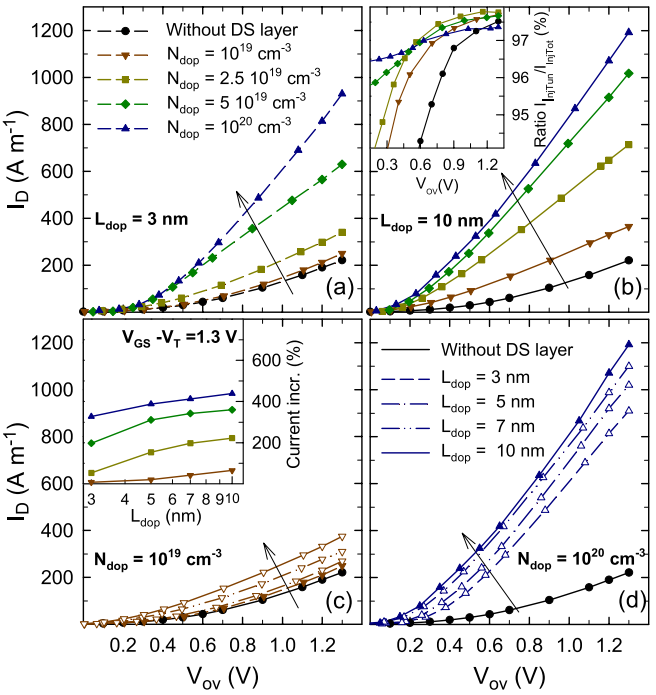

Fig. 2. Drain current as a function of gate overdrive ($V_{\rm ov}$) with constant $L_{\rm dop}$ equal to (a) 3 nm and (b) 10 nm and several values of $N_{\rm dop}$. Arrows indicate the increase of $N_{\rm dop}$. Labels of (b) are the same as in (a). Transfer characteristics as a function of $V_{\rm ov}$ with constant $N_{\rm dop}$ equal to (c) 10^{19} cm^{-3} and (d) 10^{20} cm^{-3} and several values of $L_{\rm dop}$. Arrows indicate the increase of $L_{\rm dop}$. The line type of labels in (c) are the same as in (d). Inset of (b): injected tunneling to total injected current ratio for several values of $N_{\rm dop}$ and $L_{\rm dop} = 10$ nm. Inset of (c): percentage of the current increase as a function of $N_{\rm dop}$ and $L_{\rm dop}$ for a fixed $V_{\rm ov} = 1.3$ V taking as a reference the device without DS. The drain-to-source bias is equal to 2 V.

3 and 10 nm. For this initial discussion, the smallest and the largest values of $L_{\rm dop}$ are shown. The increase of $N_{\rm dop}$ produces an improvement in the drain current value due to the additional curvature in the conduction band close to the source contact that gradually narrows the tunneling path when increasing $N_{\rm dop}$. The primary consequence is an increase of the injection by quantum tunneling, as pointed out in [17], [20], [21], and [24]. In addition, it produces a large accumulation of majority carriers (that under pinchoff conditions grows up in the whole channel but mainly in the DS region adjacent to the source contact), contrarily to what happens in the triode regime, where the accumulation occurs symmetrically on the two Schottky regions [37].

The minimum doping to obtain a significant improvement in the current (as compared to a device without DS) is 10^{19} cm^{-3}; for 5×10^{18} cm^{-3} (not shown), we obtain practically identical results as for the device without DS for all the $L_{\rm dop}$ values. Consequently, the range of doping that effectively increases the current varies from 10^{19} to 10^{20} cm^{-3}; at this upper limit, certain saturation begins to be detected. Inset of Fig. 2(b) shows the percentage of tunnel injected current over the total injected current at the source as a function of $V_{\rm ov}$ for several devices with different $N_{\rm dop}$ and fixed $L_{\rm dop}$ value equal to 10 nm. For the two largest $N_{\rm dop}$ studied, the Schottky effect can be clearly identified, reducing back the percentage of injected tunneling current and increasing the thermionic

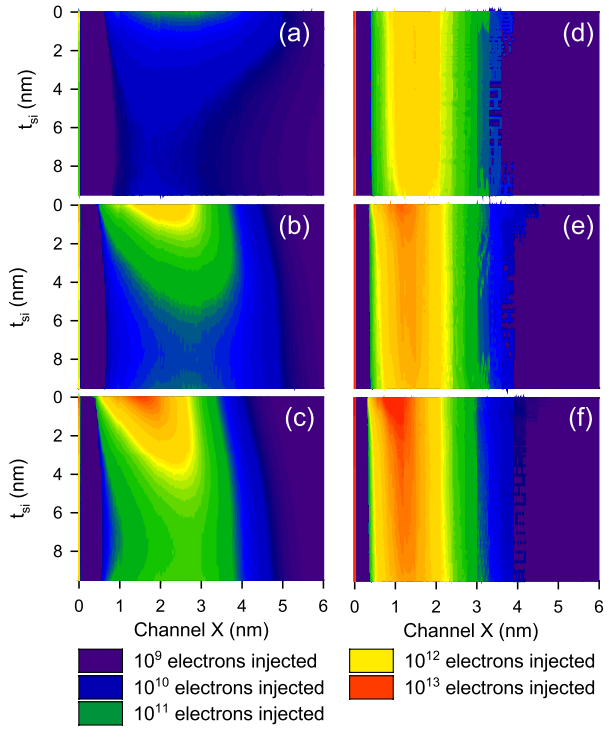

Fig. 3. Contour graphs of the distribution of carrier injection by quantum tunneling at the source contact [from 0 to 6 nm in the x-axis and 0 to 10 nm in the y-axis (see Fig. 1)]. (a)-(c) Results for a device without DS for V_{ov} 0.2, 0.8, and 1.2 V, respectively. (d)-(f) Results for a device with DS ($L_{dop} = 5$ nm and $N_{dop} = 2.5 \times 10^{19}$ cm^{-3}) and identical gate voltages.

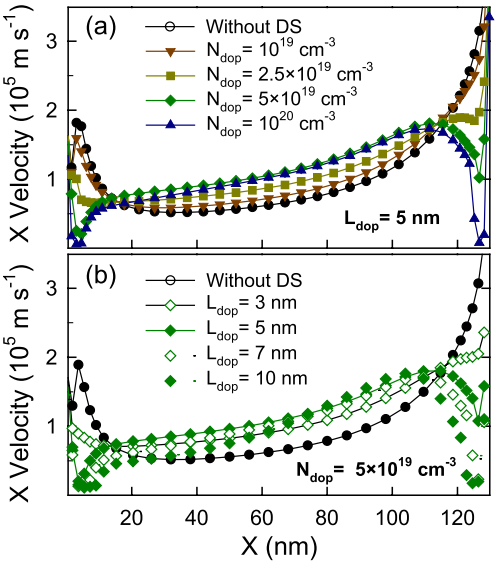

Fig. 4. (a) and (b) Profile of average longitudinal carrier velocity at $V_{DS} = 2$ V and $V_{GS} - V_T = 1.0$ V for different values of N_{dop} and $L_{dop} = 5$ nm and for constant $N_{dop} = 5 \times 10^{19}$ cm^{-3} and several L_{dop}. The values shown correspond to the average values in the whole active region properly weighted by the electron concentration along the vertical y-axis, as explained in [34].

injection percentage as both N_{dop} and V_{ov} are augmented. Fig. 2(c) and (d) shows the transfer characteristic for several values of L_{dop} considering constant N_{dop} of 10^{19} cm^{-3} and 10^{20} cm^{-3}, respectively. The increase of L_{dop} maintaining a constant value of N_{dop} also produces an enhancement of the drain current but to a lesser extent than when N_{dop} is modified. Inset of Fig. 2(c) represents the percentage of the current increase (taking as a reference the device without DS) and is displayed simultaneously as a function of the two main features of the DS layer (N_{dop} and L_{dop}) for the largest gate overdrive considered. A negligible dependence of the current with L_{dop} for a single N_{dop} value considered (equal to 10^{20} cm^{-3}) was shown in [18]; this fact can be attributed to the lack of consideration of an underlap region in that case. For the sake of simplicity to evaluate the influence of a DS layer as compared with a device without it, henceforth we focus mainly on keeping one parameter constant (to an intermediate value: $N_{dop} = 5 \times 10^{19}$ cm^{-3} or $L_{dop} = 5$ nm) while varying the other.

Fig. 3 shows the injection maps for a device without DS (left) and a device with DS of $N_{dop} = 5 \times 10^{19}$ cm^{-3} and $L_{dop} = 5$ nm (right) and three different values of the gate overdrive voltage [from top to bottom: 0.2 (near threshold conditions), 0.8, and 1.2 V] with a constant V_{DS} of 2 V.[1] In the device without DS, the injection of carriers is strongly located in the upper part of the active layer and in the first few nanometers of the underlap region. When V_{ov} augments, the amount of injected carriers strongly increases [inset of Fig. 2(b)], and the injection spreads toward the channel [Fig. 3(b) and (c)]. When the DS layer is considered, the spatial distribution of injected carriers is remarkably modified. As can be seen in Fig. 3(d)–(f), the injection takes place along the whole active layer constituted by the silicide-channel interface at the source, with a slightly higher intensity in the upper part. Similar effects were observed in [38] and [39].

The incorporation of a DS layer has important consequences on the redistribution of the internal potential inside the device. First, the depletion region of the Schottky contact narrows down with the rise of N_{dop}, strengthening the longitudinal electric field adjacent to the contact (just in the first 2–3 nm). However, in the next few nanometer, there is an important reduction of the electric field (not shown in the graphs), which becomes even of the opposite sign for the largest N_{dop} and L_{dop} considered. This slows down the carriers and reduces the drift velocity in the DS region, as shown in Fig. 4, producing a significant accumulation of carriers (in accordance to the results shown in [18]). In the rest of the channel, the longitudinal field increases and, as a consequence, the carriers preserve a greater longitudinal velocity in most of the middle part of the channel as we increase the DS doping and length, while the overshoot phenomena have less importance in the regions close to the Schottky contacts [Fig. 4(a)]. This points out to reduced carrier mobility degradation in DS devices. For the considered gate length, the average longitudinal velocity of the carriers in the whole channel is almost linearly reduced with the N_{dop} or L_{dop} increment. This is mainly due to the drastic velocity reduction at the end of the channel when the DS layer is included. For instance, at a constant L_{dop} of 5 nm, the average drift velocity reduces from 1.34×10^5 m s^{-1} (in the device without DS) down to 0.811×10^5 ms^{-1} for

[1]Fig. 3 only shows field effect injection, since thermionic processes occur just at the silicide/silicon interface.

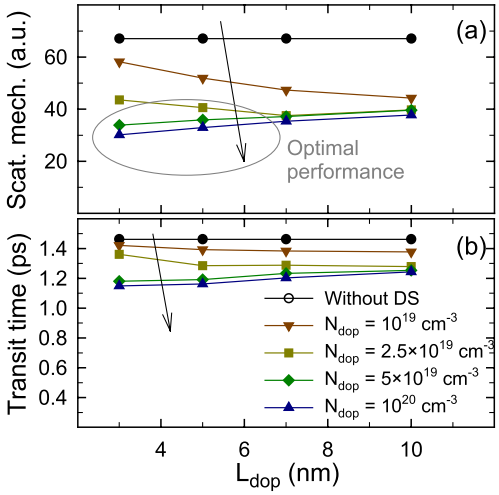

Fig. 5. (a) Total isotropic scattering mechanisms undergone by the carriers. (b) Average values of the transit time of the carriers in the channel, respectively, as a function of $N_{\rm dop}$ values and constant $L_{\rm dop}$ for $V_{\rm GS} - V_T = 1.0$ and $V_{\rm DS} = 2$ V.

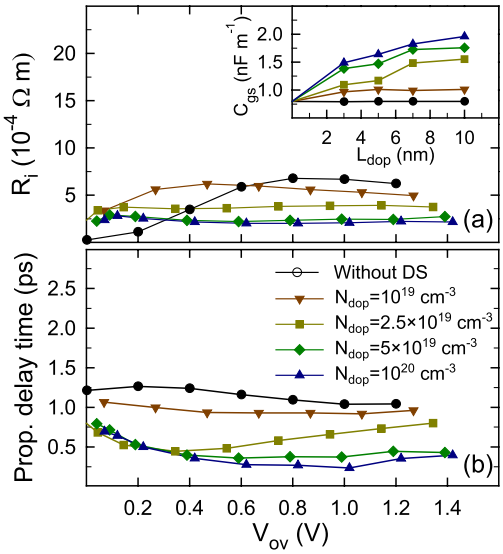

Fig. 6. (a) Intrinsic channel charging resistance R_i and (b) transconductance propagation delay time τ as a function of the gate overdrive and $V_{\rm DS} = 2$ V, for several $N_{\rm dop}$ values and constant $L_{\rm dop}$ of 5 nm. Inset: $C_{\rm gs}$ capacitance as a function of $L_{\rm dop}$ and several $N_{\rm dop}$ values for a constant $V_{\rm DS} = 2$ V and gate overdrive $V_{\rm GS} - V_T$ of 1 V.

$N_{\rm dop}$ equal to 10^{20} cm^{-3}. It must be considered that drain-induced barrier thinning and the ambipolar transport, although not relevant for the gate length and bias considered, could play an important role for gate lengths down to 30 nm.

A further inspection of the quantities related to the stochastic movement of electrons in the channel (transit time, average traveled length, and so on) has been performed. Fig. 5(a) shows the average number of scattering events suffered by one electron crossing the channel. In a device without DS, once the electrons are injected at the source, they spread in a 2-D movement toward the channel with wide angles, suffering a nonnegligible number of average scatterings inside the channel (a total of 66 isotropic scattering events, outlining the channel as a strongly diffusive framework). However, when a DS layer is included and $N_{\rm dop}$ increases, a drastic fall (nearly 50%) of phonon scattering mechanisms occurs, obeying to a reduced average carrier energy mainly at the end of the channel (i.e., much less hot carrier effects). This fact, together with a more uniform injection in the contact (Fig. 3), gives rise to a higher directionality of electron transport in the longitudinal direction, which can be improved for medium or largely doped DS layers. As an example, the average distance traveled by the carriers in the vertical direction is reduced from 377 nm in the device without DS down to 193 nm in the device with a DS of $N_{\rm dop}$ of 10^{20} cm^{-3} and $L_{\rm dop}$ of 5 nm. This fact in turn affects also the transit time [Fig. 5(b)] of the electrons traveling across the channel, which is reduced depending mainly on $N_{\rm dop}$. In addition, the mean free path of carriers is enlarged from 5.52 nm for the device without DS up to 8.53 nm for a DS device with $L_{\rm dop}$ equal to 5 nm and $N_{\rm dop}$ of 5×10^{19} cm^{-3}.

The gate-to-source capacitance, $C_{\rm gs}$, shows (for all the $N_{\rm dop}$ and $L_{\rm dop}$ values) dependence with $V_{\rm GS}$ similar to that of devices without DS [29]. The beneficial reduction of $R_{\rm ON}$ (a parameter that is inversely proportional to the charge in the channel) provided by the DS layer [37] is accompanied by a reinforcement of the capacitive phenomena [see inset of Fig. 6(a)]. The $C_{\rm gs}$ capacitance increases both with $L_{\rm dop}$ and $N_{\rm dop}$ (agreeing with the experimentally observed augmentation in [19]) due to the larger accumulation of carriers in the DS layer area located between source and gate terminals, and so the increase in carrier concentration is locally enhanced as a response of a gate voltage step.

The nonquasi-static parameters R_i (intrinsic channel resistance) and τ (the transconductance delay time) are shown in Fig. 6 as a function of $V_{\rm ov}$ for $V_{\rm DS} = 2$ V. The results indicate that increasing $N_{\rm dop}$ (for $V_{\rm ov} > 0.6$ V), it is possible to reduce the values of R_i in a factor >3. The increase of the DS layer doping produces a faster response of the charge within the channel (indicated by smaller delay times), which is due to the fine tuning of the quantum transmission coefficient that controls the injection of carriers. The variation of τ with $L_{\rm dop}$ is strongly minimized by the presence of the doped layer regardless of its width (not shown in the graphs). The values of τ are clearly below the values obtained for a conventional bulk MOSFET [32] and are also lower that the previously shown average transit time of the carriers in the channel.

An outstanding enhancement of the transconductance, g_m, is observed for the DS devices, with values that double those for the device without DS for intermediate values of $N_{\rm dop}$ and $L_{\rm dop}$ or can even quadruple them for $L_{\rm dop}$ of 5 nm and the largest $N_{\rm dop}$ considered [Fig. 7(a)]. For each simulated $N_{\rm dop}$ and for any value of $L_{\rm dop}$ above 7 nm, an upper limit in the increasing tendency of g_m was obtained. In addition, our transconductance results are in good qualitative agreement with those presented in n-type [19], [24] and also in p-type transistors with comparable geometric characteristics [17]. In spite of the nonconvenient $C_{\rm gs}$ growth, the g_m improvement yields the cutoff frequency (f_T) values of DS devices to be relative larger than the ones of the device

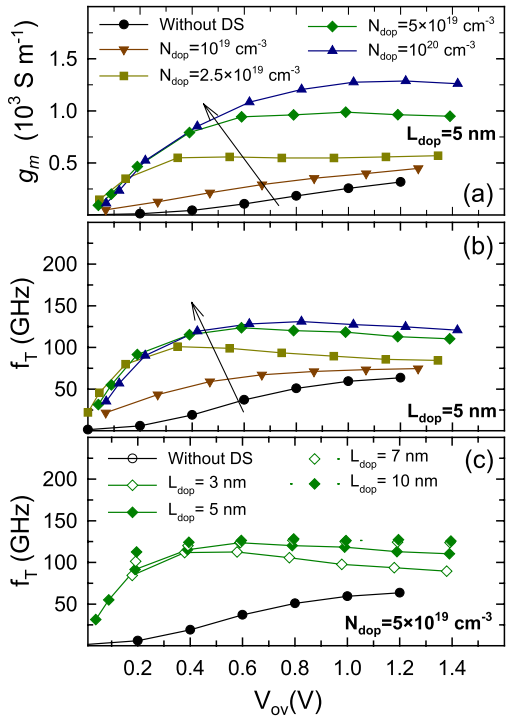

Fig. 7. (a) Transconductance as a function of $V_{GS} - V_T$ and $V_{DS} = 2$ V, for several N_{dop} values and constant L_{dop} of 5 nm. (b) Cutoff frequency as a function of the gate overdrive and $V_{DS} = 2$ V, for several N_{dop} values and constant length 5 nm. (c) Cutoff frequency for identical voltage conditions of (a) for a constant $N_{dop} = 5 \times 10^{19}$ cm^{-3} and several L_{dop} values.

without DS [Fig. 7 (b)]. As N_{dop} is augmented (for a constant L_{dop}), an important rise of f_T is reached, as can be seen in Fig. 7(b). For N_{dop} values $>10^{20}$ cm^{-3}, no significant increase of f_T was observed. An increase of L_{dop} can also be slightly beneficial to improve f_T, mainly for the lower values of N_{dop} [Fig. 7(c)]. For the SB-MOSFET without DS, the maximum value of the cutoff frequency, 63 GHz, is obtained for a gate overdrive of 1.2 V. In addition, an interesting displacement of the V_{ov} value for which the f_T reaches its maximum appears in the DS transistors, first toward lower V_{ov} value (for N_{dop} from 0 to 2.5×10^{19} cm^{-3}) and finally toward higher V_{ov} values (for $N_{dop} > 2.5 \times 10^{19}$ cm^{-3}). This fact, attributed to the increase of the C_{gs} capacitance for large V_{ov} values, can be extremely beneficial for the design of low-power applications, and causes, for instance, that a f_T maximum value of 124 GHz for N_{dop} 2.5×10^{19} cm^{-3} takes place for V_{ov} of about only 0.6 V. The increase of the DS layer doping causes a doubling on the frequency performance of the DS device (compared with the without DS counterpart) while reducing the power consumption.

Power dissipation is an important property of a device that affects feasibility, cost, and reliability. Despite being a parameter valued primarily for studying the behavior of a transistor under switching conditions, the PDP can be considered also as a quality measure of the device and, in our case, can be very useful from the point of view of optimizing the DS layer. Fig. 8 shows the results obtained for the PDP for constant V_{DS} condition that ensures a fair comparison. This FoM indicates that the devices are faster, while maintaining reasonable power

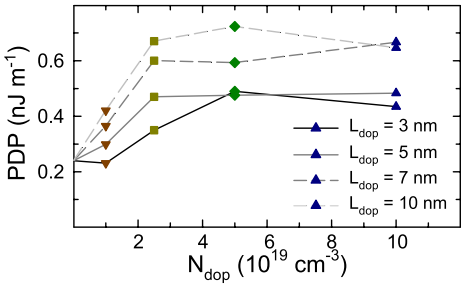

Fig. 8. PDP FoM of the DS-SB-MOSFET as function of N_{dop} for different values of L_{dop} and $V_{GS} - V_T = 1$ V and $V_{DS} = 2$ V. The delay time in the PDP is the nonquasi-static parameter of SSEC shown in Fig. 6(b).

consumption, if N_{dop} and L_{dop} are <5 nm and 5×10^{19} cm^{-3}, respectively. However, larger values of N_{dop} that efficiently enhance g_m and reduce the average transit time of the carriers are not desirable from the point of view of the PDP FoM due to the larger power consumption, which explains the trends observed in Fig. 8.

IV. Conclusion

An EMC simulator has been used to study the impact of incorporating a DS layer on charge transport and the high-frequency performance of a SB-MOSFETs device. When a DS layer is considered the injection process is modified, being more homogeneous along the whole contact interface. The increase of N_{dop} or L_{dop} also leads to an improvement of the 1-D of carrier transport along the active region, accompanied by a reduction of the hot carrier effects at the end of the channel. While most benefits are obtained considering a more doped DS layer (e.g., for N_{dop} equal to 5×10^{19} cm^{-3} the transit time could be reduced a 17% and the average traveled path a 35%), increasing L_{dop} has some constrains, since very high L_{dop} values could penalize the transit time or generate more scattering events. Although we observed a strong improvement of the transconductance and for the cutoff frequency, a reduced enhancement is obtained due to the increase of the gate-to-source capacitance when N_{dop} or L_{dop} increase. However, the modification of the parameters of the DS layer becomes critical for the nonquasi-static parameters of the SSEC: reduced values of the intrinsic channel resistance, in a factor >3 are accounted (for the N_{dop} values considered), and lower values of the delay time mainly when N_{dop} is increased. This leads to adequate power-delay product values in spite of the very large current increase for large N_{dop} and low L_{dop} values, determining that using a highly doped (over 5×10^{19} cm^{-3}) and thin DS layer (lower or equal to 5 nm) is a suitable way to significantly improve the performance of SB-MOSFETs for RF applications.

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María Jesús Martín received the B.S. and Ph.D. degrees in physics from the University of Salamanca, Salamanca, Spain, in 1992 and 1996, respectively.

Her current research interests include Monte Carlo modeling of electronic transport, dynamic characterization, noise in RF range of submicrometer silicon devices and nonconventional MOSFETs, and simulation and analysis of graphene materials.

Carlos Couso received the Industrial Engineering and Materials Engineering degrees from the University of Salamanca, Salamanca, Spain, in 2009 and 2011, respectively. He joined the Department of Applied Physics with the University of Salamanca as a Junior Researcher in 2012. He is currently pursuing the Ph.D. degree with the REDEC Group, Autonomous University of Barcelona, Barcelona, Spain.

Elena Pascual received the B.S. and Ph.D. degrees in physics from the University of Salamanca, Salamanca, Spain, in 2005 and 2010, respectively.

She has been an Assistant Professor with the University of Salamanca since 2014. Her current research interests include Monte Carlo modeling of electron transport in silicon and graphene devices, including investigation of electronic noise processes of Schottky barrier MOSFETs.

Raúl Rengel received the B.S. and Ph.D. degrees in physics from the University of Salamanca, Salamanca, Spain, in 1997 and 2003, respectively.

His research activity has been focused on the Monte Carlo simulation of the high-frequency properties of silicon devices. His current research interests include the development of simulators for the study of graphene and 2-D materials.