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Towards the nanoscale: influence of scaling on the electronic transport and small-signal behaviour of MOSFETs

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Abstract
In this work, the influence of downscaling bulk MOSFETs below the 100 nm range on their static and dynamic behaviour is analysed by means of a particle-based Monte Carlo simulator. Internal transport conditions are investigated throughout the extensive information provided by numerical simulations (electric fields, concentration, velocity and energy of carriers, energy bands, etc), and a physical interpretation is given to the dynamic behaviour observed. Results show that even when the most favourable downscaling conditions are considered (that is, following the constant field scaling rules), significant two-dimensional electrostatic effects, together with reduced gate control, lead to the degradation of important figures of merit such as gate-to-source capacitance, transconductance or maximum oscillation frequency. Conventional MOSFET geometries are therefore near to a limit when reaching gate lengths of 50 nm, and the use of alternative solutions is necessary in order to maintain the proper electrostatic behaviour of a 'well-tempered' transistor.

1. Introduction

The outstanding progress of silicon technologies in the last few decades has been achieved, to a great extent, through the scaling of MOSFET devices. The continuous reduction of the dimensions of the transistors has provided enormous benefits in both digital and analogue applications (i.e. higher number of transistors per chip, faster switching speed, improved RF performance, etc) [1, 2]. Although many alternatives to traditional devices have been proposed in the last few years, such as silicon-on-insulator devices, double gate MOSFETs, Schottky barrier source/drain MOSFETs, or other different approaches such as carbon nanotube FETs [3–5], bulk silicon transistors are still the mainstream devices in the market [6]. Therefore, it is necessary to evaluate the effects of downscaling on the behaviour of the devices when approaching the nanoscale, and much effort has been made in the last few years to maintain the trend of MOSFET downsizing in the future (see, e.g., [7]). Although advanced conventional MOSFETs with 15 nm gate lengths have been already demonstrated [8], in general the main research and development efforts are still focused on the optimization and physical comprehension of the behaviour of sub-100 nm structures.

When dealing with downscaling issues, the parameters of the geometry are usually modified in a tailored fashion in order to fulfil the specific requirements of a given application. Nevertheless, in the literature several scaling rules affecting the main parameters of the device topology have been proposed. Among them we can mention the following: the constant field (CF), the constant voltage (CV) and the quasi-constant voltage (QCV) scaling methods [9–12]. Table 1 shows the different scaling rules for each one of these proposed schemes. From the theoretical point of view, considering the CF scheme is the most interesting option, since in this case the electrostatic conditions (electric fields, depletion regions, etc) inside the device should not be modified when the dimensions are shrunk, and the transport properties should stay similar for the different MOSFET generations. Although this scaling method has not been strictly followed by the industry, is has been considered as an essential blueprint in evaluating the scaling roadmap over the last two decades [13]. Identifying the possible problems appearing within this ideal framework can be very useful in

Table 1. Summary of different 'classical' scaling methods.

Magnitude	CF	CV	QCV
Dimensions	$1/\kappa$	$1/\kappa$	$1/\kappa$
Voltage	$1/\kappa$	1	$1/\kappa^{1/2}$
Substrate doping	κ	κ	κ
Oxide thickness	$1/\kappa$	$1/\kappa^{1/2}$	$1/\kappa$

order to help designers in their quest for improved nanoscaled transistors.

This paper addresses an investigation of the consequences of scaling bulk MOSFETs beyond the 100 nm range, by means of an ensemble Monte Carlo simulator [14], focusing on the study of the transport properties and dynamic behaviour at RF and microwave frequencies. Taking a 250 nm gate length MOSFET structure as the starting point, the CF scaling rules are considered, and progressively smaller structures with gate lengths corresponding to actual technology nodes (130, 90 and 60 nm) [6] are studied in depth. Many authors have previously investigated transport phenomena in deep submicron MOSFET devices by means of EMC simulators (see, e.g., [15–17]). Recently, the implementation of quantum effects [18] or the study of advanced ultra-small devices (i.e. low Schottky-barrier MOSFETs [19]) are receiving special attention. Other groups have studied also the dynamic behaviour of MOSFET devices based on transient EMC simulations [20] and the constant field scaling was analysed for gate lengths down to 120 nm by Ellis-Monaghan *et al* [21] by means of a particle-based simulator in order to describe the influence of hot-carrier injection in the oxide. However, to the author's knowledge, a detailed EMC study of the consequences of constant field scaling on the high-frequency dynamic behaviour (with small-signal equivalent circuit parameters evaluated directly from transient EMC simulation) of sub-100 μm has not been performed up to date. With the information provided by the simulator, is it possible to provide a physical insight to the results obtained for high-frequency dynamic figures of merit and also to detail the modifications observed in the charge transport conditions.

The paper is organized as follows. In section 2, the simulated structures are described, together with some comments about the EMC procedure. In section 3, the transfer characteristics and important internal quantities such as electric fields, concentration and energy of carriers, energy bands, etc are discussed. The results for the main parameters of the small-signal equivalent circuit (SSEC) are presented and examined in section 4. Finally, the main conclusions of our work are reported.

2. Monte Carlo simulator and structure of the devices under analysis

A schematic diagram of the simulated n-channel MOSFET structures is shown in figure 1. The physical and geometrical parameters of the smaller devices have been obtained from the ones of the 250 nm transistor following the CF scaling rules, which were shown in table 1. As mentioned above, we focused on ideal structures with gate lengths of 130, 90 and 60 nm; the corresponding values of the scaling factor κ are 1.93, 2.78 and 4.17, respectively. The main parameters of the devices are shown in table 2.

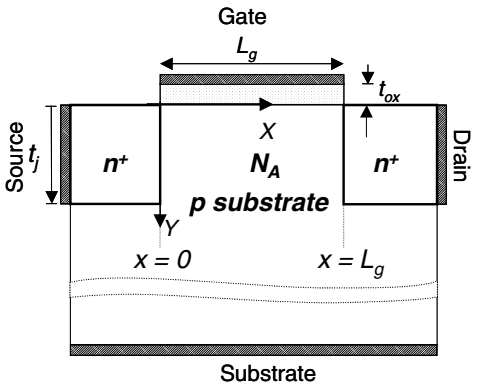

Figure 1. Schematic diagram of the simulated devices. Parameters for each structure are given in table 2.

Table 2. Main topology parameters (obtained following the CF scaling method) for the structures under study.

L_g (nm)	t_{ox} (nm)	N_A (10^{23} m^{-3})	n^+ (10^{23} m^{-3})	t_j (nm)	κ
250	8.25	4	10	100	1
130	4.3	7.7	20	50	1.93
90	3	11	28	35	2.78
60	2	16.5	42	25	4.17

It must be remarked upon that, as noted in table 1, the ideal scaling rules impose not only the modification of the main topology parameters, but also the reduction of the bias voltages. In our case, both the drain voltage (V_{DS}) and the gate voltage (V_{GS}) for the smaller MOSFETs have been properly scaled down. Most of the results in this paper are plotted as a function of $V_{GS} - V_T$ (V_T being the threshold voltage); in this case, in the axis of the graphs the values of $V_{GS} - V_T$ for each transistor are multiplied by the corresponding κ in order to make a suitable graphical comparison between the results for the different structures.

The calculations have been carried out by means of a bipolar EMC simulator consistently coupled with a two-dimensional (2D) Poisson solver. Our simulator was successfully employed in previous works for the study of the static, dynamic and noise behaviour of different theoretical and experimental MOSFET structures [22, 23]. When dealing with the static analysis of MOSFETs, it is appropriate to consider holes in a quasi-static approximation in the resolution of the Poisson equation [24]. Nevertheless, in the case of the dynamic behaviour, one should consider the simultaneous self-consistent dynamics of both types of carriers in order to capture the influence of substrate holes on the high frequency dynamic response of the devices, particularly when dealing with the correct determination of the drain-to-source capacitance. Thus, in our case, both electrons and holes are simulated as particles. The devices are divided into adaptive meshes in order to solve accurately the Poisson equation in the whole device, including the gate oxide (due to the high concentration of the inversion layer the size of the meshes is smaller in the region under this oxide). The time step used to solve the Poisson equation is 1 fs, and the number of simulated particles is usually around 12 000 electrons and 25 000 holes, although these figures may vary depending on the bias point and the structure considered. A

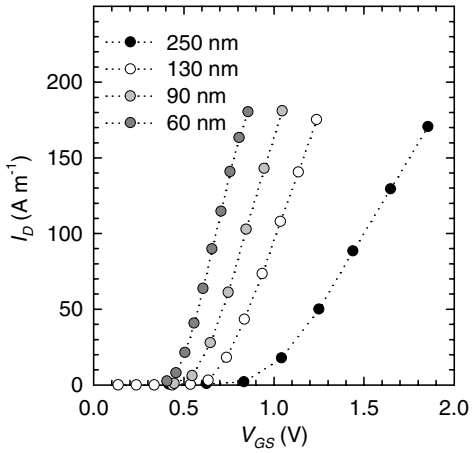

Figure 2. Transfer characteristics for the four structures. The corresponding drain voltages are 1.25, 0.65, 0.45 and 0.4 V for the 250, 130, 90 and 60 nm MOSFETs, respectively. V_{GS} is not normalized in order to emphasize the differences between the transistors.

detailed description of the conduction and valence bands in the simulator, together with the scattering mechanisms and parameters considered for electrons and holes, can be found in [25]. Room temperature was considered in the simulations. At the oxide–semiconductor interface the continuity of the displacement vector normal to the surface is take into account, whereas Dirichlet (fixed potential) conditions are applied at the four terminals. The source, drain and substrate contacts are treated as ohmic [26], being the source and substrate short-circuited. The non-simulated dimension corresponds to the total width (W) of the devices; most of the results will be shown normalized by this magnitude. Parasitic resistances and capacitances can be incorporated into the simulation results [23], although in this work they were not considered in order to check the intrinsic behaviour of the devices. Phenomena such as gate leakage (expected to be significant for t_{ox} below 3 nm [7]) or quantum effects (that affect charge transport for gate lengths below 50 nm [27]) were neglected; in this way, a direct evaluation of the possible degradation of the device performance just due to the downscaling of the topology parameters can be performed.

3. Static characteristics

The transfer characteristics (in which the applied drain voltage has been properly scaled following the CF rules) for the four devices are plotted in figure 2. A reduction of V_T is observed as the devices are scaled down (due to the corresponding higher channel doping, as shown in table 2). Moreover, a larger slope is obtained in this case, thus indicating, as a first result, a higher transconductance per unit width. In order to obtain a deeper understanding of the transport conditions inside the device, we have analysed in depth the information on the internal quantities of interest provided by the EMC simulator. As an example, in figure 3 we show a 2D contour plot for the electric field along the X dimension (longitudinal field, E_X), in the 250 nm (a), 130 nm (b), 90 nm (c) and 60 nm (d) devices for equivalent scaled bias conditions, corresponding to $(V_{GS} - V_T)\kappa = 0.25$ V and $V_{DS}\kappa = 1.25$ V.

In an ideal conventional MOSFET, the highest values of E_X should be clearly located at the drain and source junctions, whereas most of the channel should present almost negligible values of E_X as compared to the maximum values at the junctions. For the 250 nm device, this is quite well fulfilled; however, below 100 nm the important influence of the source and drain junctions leads to very high values of E_X in an important part of the conducting channel, and even for the smallest transistor the 'low-field' region disappears. It must be remarked that in the case of considering a non-scaled drain voltage, this electrical distortion is even higher. Focusing on the longitudinal electric field below the Si–SiO_2 interface (where charge transport is mainly carried out), as the dimensions are reduced a progressively increasing electric field opposing the electron movement from source to drain takes place at the beginning of the channel (reaching a value up to 50 kV cm^{-1} for the 60 nm device).

Due to these facts, the transport conditions inside the transistor are strongly affected in small devices. As an example, we have checked that the downscaling of the dimensions involves the modification of the ideal inversion layer profile of a MOSFET (figure 4), especially for the shortest devices, owing to the already commented on two-dimensional electrostatic effects. As can be observed in figure 4, for high values of the κ factor an increasing portion of the channel corresponds to the pinch-off region, and subsequently the inversion layer presents a trend to spike near the source. Important consequences are observed in some SSEC parameters, as we shall see in the following section.

The values of the average carrier energy below the Si–SiO_2 interface along the channel for the different structures are shown in figure 5, together with the corresponding values of the bottom of the conduction band at the same bias conditions as those of figure 3. The results show that for small transistors an important reduction of the peak value of the average energy is obtained (always bearing in mind the specific bias conditions considered), leading to a minor influence of hot carrier effects. We have also checked with our simulator that in this case fewer inter-valley transfers and reduced phonon scattering take place near the drain in small devices. Concerning the conduction band profile, as can be observed in figure 5(b) for high values of the scaling factor, an important increase of the barrier inside the channel is obtained (in good agreement with the observed electric field behaviour), thus indicating a regime of operation closer to a bipolar junction transistor in extremely short devices. When the dimensions are shrunk, the gate progressively loses control of the channel, and the drain becomes the dominant element on the charge transport conditions. Finally, we must mention that the results of velocity (not shown in the graphs) have demonstrated the appearance of overshoot effects near the drain for all the devices analysed; nevertheless, in the 60 nm device the velocity peak is reduced by 15% as compared to the other small-size transistors.

4. Dynamic behaviour

The ac behaviour of a MOSFET device can be represented through the complex frequency-dependent two-port admittance (Y) parameters [28]. The EMC method allows us to perform the calculation of these parameters by means of the

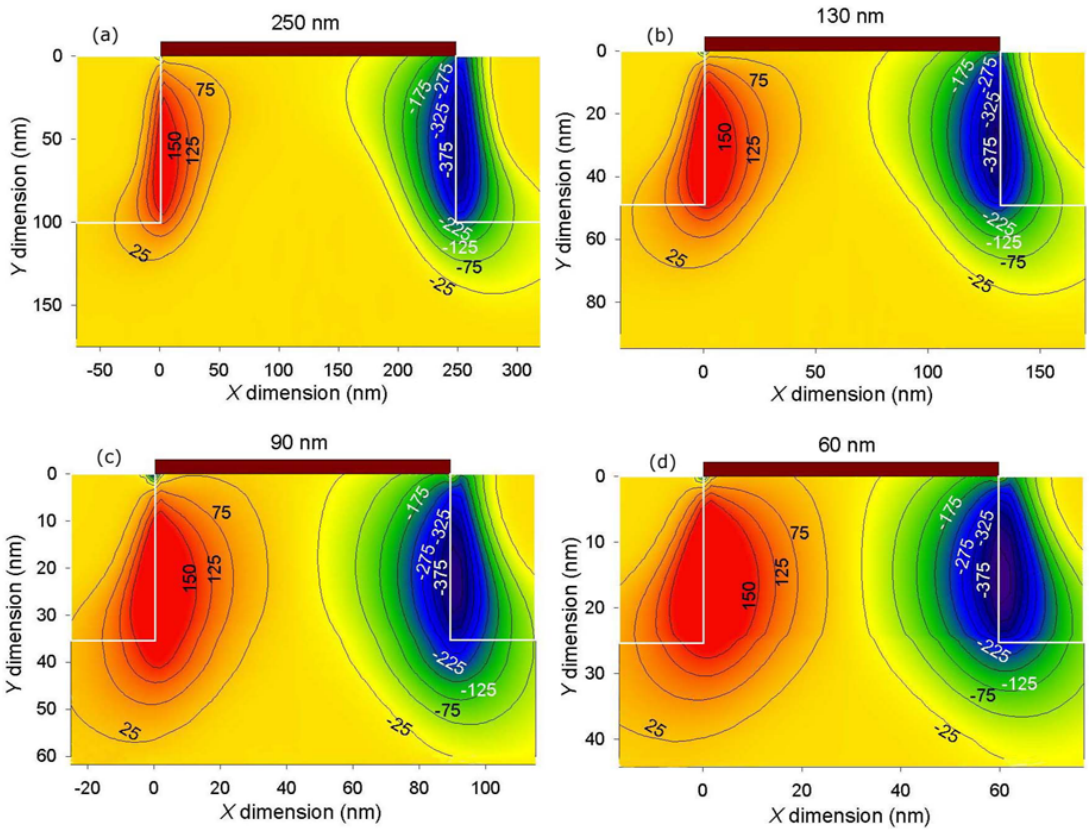

Figure 3. 2D contour plot of the electric field along the X direction for the (a) 250 nm, (b) 130 nm, (c) 90 nm and (d) 60 nm MOSFETs, with $(V_{GS} - V_T)\kappa = 0.25$ V and $V_{DS}\kappa = 1.25$ V.
(This figure is in colour only in the electronic version)

following procedure. Starting from a stationary bias point, small step voltage perturbations are applied separately at the gate and drain terminals (ΔV_{GS} and ΔV_{DS} respectively), and the simulation proceeds until the new stationary conditions are reached. Meanwhile, the instantaneous values of gate and drain current for each time step are recorded, and this set of data can be treated mathematically by means of Fourier transformation in order to obtain the four Y parameters [29]. It must be remarked that special care must be considered when choosing the values of the applied voltage steps in order to avoid problems related to numerical and physical noise, and possible harmonic generation. As an example, for the bias point corresponding to $V_{GS} = 1.0$ V and $V_{DS} = 1.25$ V in the 250 nm device, ΔV_{GS} and ΔV_{DS} have been chosen to be equal to 62.5 and 150 mV, respectively.

Once the Y parameters are determined, one can choose a small-signal equivalent circuit (SSEC) representation in order to provide a more physical interpretation of the dynamic performance of the transistors. In our case, we have chosen the SSEC shown in figure 6, which is usually employed for FET devices [30]. It incorporates the important non-quasi-static parameters R_i (channel charge resistance) and τ (transconductance delay) in order to allow a correct description of the high-frequency dynamics of the device in the saturation regime. The results shown in this section correspond to the RF and microwave values of the SSEC parameters.

The small-signal capacitances (normalized by the total oxide capacitance C_{OX}) for the different devices are plotted in figure 7 as a function of the normalized gate overdrive voltage. In an ideal MOSFET, for a fixed V_{DS} the gate-to-source (C_{GS}) capacitance must take the highest values in saturation (theoretically $2/3C_{OX}$) [31], since in this case the source end of the channel accounts for the larger part of the inversion charge. Nevertheless, as V_{GS} is increased and the device approaches the triode regime, the difference between C_{GS} and the gate-to-drain (C_{GD}) capacitance tends to be reduced since the inversion charge is more balanced along the channel. The drain-to-source (C_{DS}) capacitance should remain almost constant (and clearly lower than C_{GS} in saturation). As can be observed, the 250 nm MOSFET is in quite good agreement with this ideal behaviour. The CF scaling predicts that all the normalized SSEC capacitances should remain constant; in our case, this prediction is confirmed, with the exception of the values for C_{GS}, for which an important drop is obtained as the dimensions are shrunk (in the 60 nm device the maximum value of C_{GS} is 45% smaller than in the 250 nm transistor). The reason for this reduction in the expected values of C_{GS} can be found in the profiles of electron concentration previously commented on. In very small transistors, the drain–substrate junction significantly affects the shape of the inversion layer near the source, yielding a spike in the electron concentration just beside the source. The variation of inversion charge with the gate voltage is much lower than in the case of the bigger devices where the inversion layer profile is much more homogeneous. The end result is an important reduction of C_{GS} and a comparative stronger influence of C_{DS}. This leads

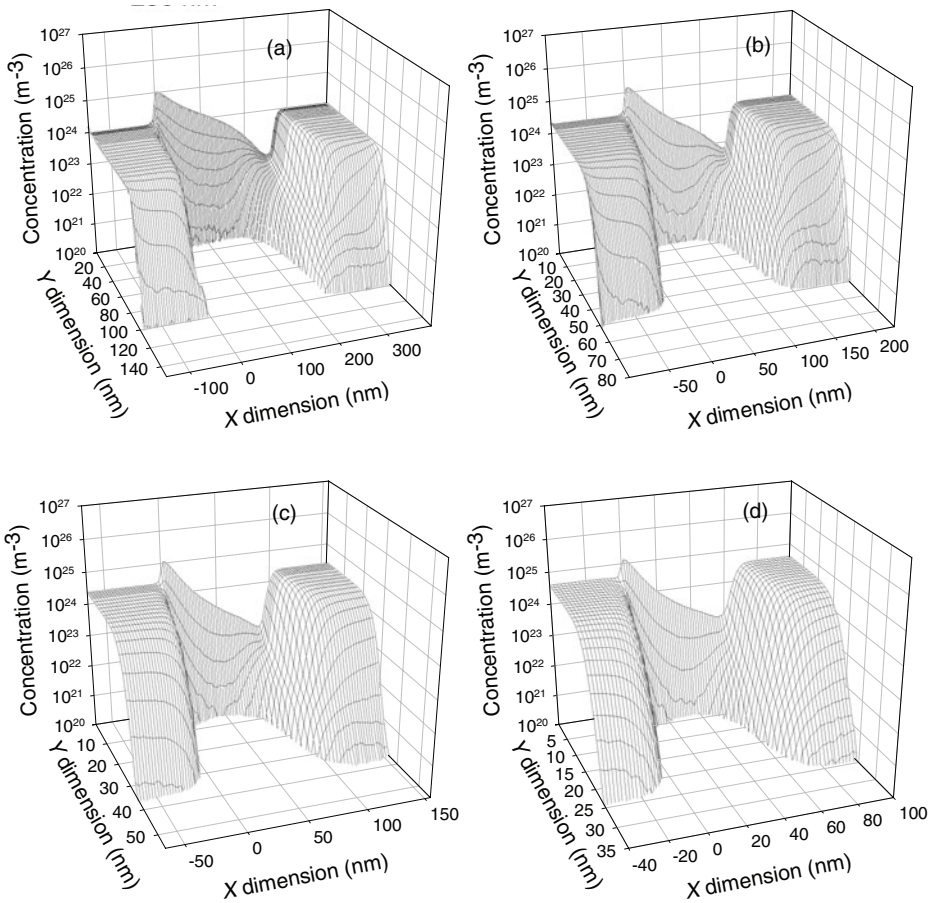

Figure 4. Electron concentration for the (a) 250 nm, (b) 130 nm, (c) 90 nm and (d) 60 nm MOSFETs, with $(V_{GS} - V_T)\kappa = 0.25$ V and $V_{DS}\kappa = 1.25$ V.

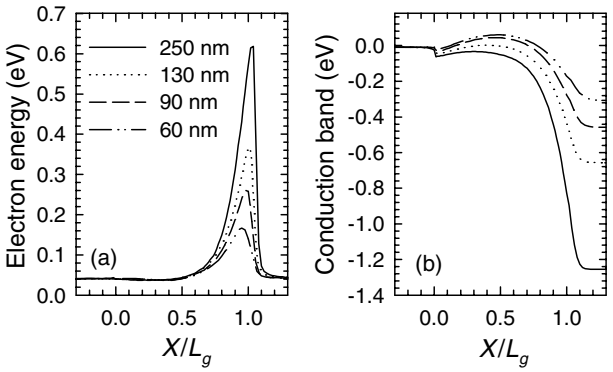

Figure 5. (a) Energy of carriers below the Si–SiO_2 interface and (b) conduction band profile for the different structures. $(V_{GS} - V_T)\kappa = 0.25$ V and $V_{DS}\kappa = 1.25$ V.

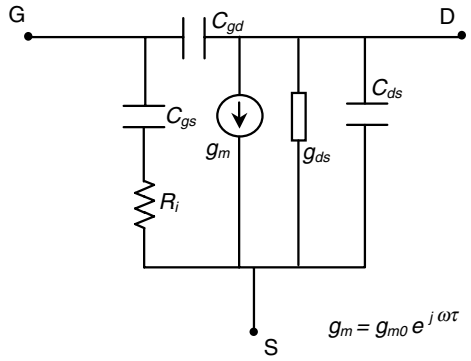

Figure 6. Schematic diagram of the small-signal equivalent circuit (SSEC) considered.

to an almost capacitor-like behaviour of the bulk MOSFET, which confirms the important loss of gate control; the optimum operation of the device in saturation is therefore strongly limited to the small bias range where C_{GS} is higher than C_{DS}.

R_i and τ are shown in figure 8 as a function of the gate biasing. A reduction of both non-quasi-static parameters is observed as the scaling factor is increased. When the gate length is reduced, on the one hand the lower values of C_{GS} and R_i show that the charge at the source end of the channel is able to respond much faster to the variation of V_{GS} (which is reflected in the decrease of the charging capacitance R_i associated to C_{GS}). On the other hand, the reduction in τ indicates that the drain current responds much faster to high-frequency variations in the gate potential in short devices.

The transconductance per unit width g_m, together with the output conductance g_{ds}, are shown in figure 9. First of all it must be noted that the increase of g_m previously envisaged in the transfer characteristics is confirmed in the dynamic calculation. Nevertheless, it is worth mentioning that a drop in the expected values for the shortest devices appears, since while the maximum values obtained are around

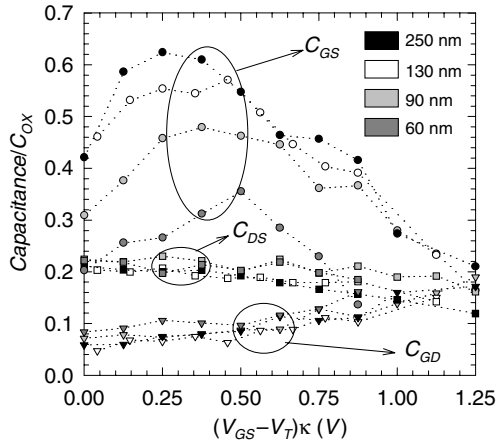

Figure 7. SSEC capacitances in the four devices as a function of $(V_{GS} - V_T)\kappa$. V_{DS} is 1.25, 0.65, 0.45 and 0.4 V for the 250, 130, 90 and 60 nm transistors, respectively.

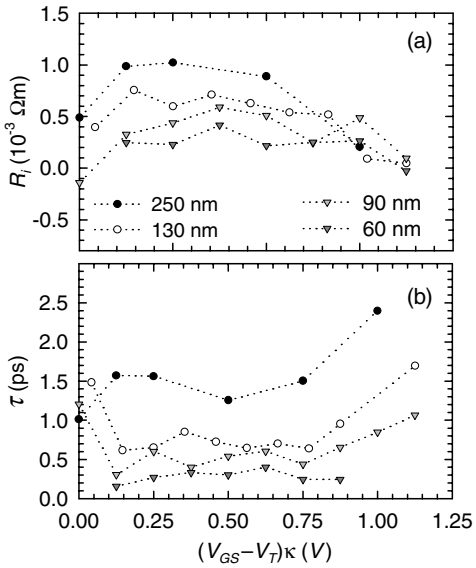

Figure 8. (a) R_i and (b) τ as a function of $(V_{GS} - V_T)\kappa$.

400 S m^{-1} for the 60 nm MOSFET, scaling rules would predict almost a doubling for this device, which is near 800 S m^{-1}, taking as a reference the results for the 250 nm device. The main reason for this fall is the increase of the channel energy barrier previously commented on; carriers are allowed to surpass the channel with a reduced probability and therefore the saturation current per unit width is lower-than-expected in the smallest devices. Moreover, the increase of channel doping affects negatively the minority carrier mobility inside the channel. The combination of both facts leads to the observed degradation in the expected values for g_m.

The intrinsic cut-off frequency f_T is represented in figure 10(a). Significantly higher values are obtained for the smaller transistors, since in this case the drop in the expected values for g_m is partially compensated for by the reduction in the normalized C_{GS}, thus leading to a significant increase for this figure of merit and keeping as reasonable as possible the CF predictions. Nevertheless, one must bear in mind the previous comments concerning the bias ranges useful for

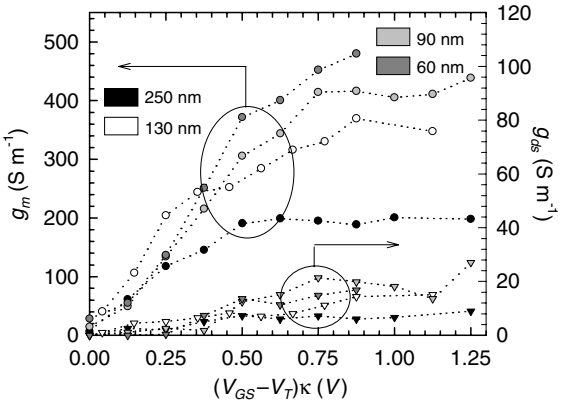

Figure 9. g_m and g_{ds} for the different devices in the same CF scaling bias conditions.

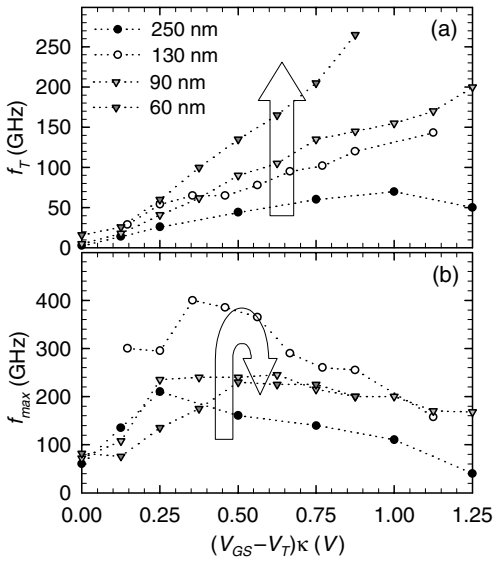

Figure 10. (a) f_T and (b) f_{max} as a function of $(V_{GS} - V_T)\kappa$.

a satisfactory transistor behaviour, which in fact is limiting considerably the performance of small MOSFETs. I.e., for the 60 nm transistor the values of C_{GS} are only significantly higher than those of C_{DS} for a gate bias voltage between 0.45 and 0.55 V ($(V_{GS} - V_T)\kappa$ between 0.3 and 0.7 V), and in this case the highest value of the cut-off frequency provided in an acceptable operating regime is near 150 GHz, which is just slightly higher than the values provided by the 90 nm MOSFET. Regarding the maximum oscillation frequency f_{max}, the results are plotted in figure 10(b). First of all, it must be noted that the values shown correspond to purely ideal devices, where the effect of parasitic contact resistances has not been incorporated into the calculation. Therefore, the results for f_{max} must be analysed from a qualitative point of view, this is, as an indicator of the expected behaviour taking as the starting point the measurements for a given 'long' device. In our case, an important degradation of this figure of merit for gate lengths below 100 nm can be observed. As a consequence of the behaviour observed for the gate-to-source capacitance, our results for the C_{GS}-to-C_{GD} ratio are lower than expected in that bias range, thus explaining the important reduction obtained for f_{max}. This shows an important loss of power gain in this case,

which confirms the poor yield of the smallest bulk MOSFETs due to the weak transistor action.

The structures investigated in this work correspond to ideal, self-aligned gate devices. In fabricated MOSFET transistors, the highly doped source and drain regions diffuse under the gate, leading to the appearance of the so-called *overlap* regions [31]. The length of these overlap regions is directly related to the fabrication process. Even when the advances of fabrication techniques for each transistor generation lead to smaller overlap lengths, it has been shown that the increasing influence of overlap capacitances as the gate length is reduced (in particular raising the ratio between the Miller capacitance and the total gate-to-source input capacitance) may lead to an important degradation of f_T and f_{max} together with an additional loss of channel charge control by the gate with respect to those expected for the intrinsic transistor [32]. Therefore, in addition to the poorer RF behaviour due to electrostatic effects already found in this work, for fabricated devices with similar geometries to those studied in this paper the overlap effects would lead to a further degradation from the ideal of the main high-frequency figures of merit.

5. Conclusions

In this work, the effects of downscaling the bulk MOSFET towards the nanoscale range on the high-frequency dynamic behaviour of the devices has been investigated by means of an ensemble Monte Carlo simulator. It has been checked that an important modification of the internal quantities (inversion layer profiles, energy bands in the channel, longitudinal electric fields, etc) exists due to the proximity of source and drain junctions and the associated 2D electrostatic effects, even when the most ideal bias conditions are imposed. These effects turn into an important constraint when the loss of gate control over the channel begins to affect the transistor action and the high-frequency performance of the devices. We have checked that for gate lengths below 100 nm the degradation of the main dynamic figures of merit from the ideal scaling forecast is significant. In particular, whereas gate-to-drain and drain-to-source capacitances agree well with the theoretical prediction, the gate-to-source capacitance is strongly reduced as the devices are scaled-down; for very small transistors, a capacitor-like behaviour from drain-to-source is obtained. Non-quasi-static parameters tend to decrease for small devices, in good agreement with their underlying physics. The values of g_m below 100 nm gate lengths are significantly lower than those expected by the CF theory. Moreover, in this case an important degradation of the maximum oscillation frequency is to be expected due to the important reduction in the C_{GS}-to-C_{GD} ratio. Furthermore, for the 60 nm MOSFET the bias-range in which the device behaves as a FET in saturation is extremely reduced as compared to bigger structures.

In summary, designers must pay special attention to the electrostatic effects inside transistors when reaching the nanoscale, because of the risk of losing a proper FET yield in a conventional bulk device. From the point of view of the dynamic high-frequency behaviour of the devices, the results presented in this work suggest that, in addition to the well-known short channel effects, bulk MOSFETs with shorter gate lengths than those studied in this paper (below 60 nm), may present severe performance limitations due to the tendency of the device to operate as a two-terminal capacitor if the design of source and drain junctions is not fully optimized.

Acknowledgments

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