Comparison Between the Noise Performance of Double- and Single-Gate InP-Based HEMTs

Beatriz G. Vasallo, Nicolas Wichmann, Sylvain Bollaert, Yannick Roelens, Alain Cappy, *Senior Member, IEEE*, Tomás González, *Senior Member, IEEE*, Daniel Pardo, and Javier Mateos

***Abstract*—The noise performance of InAlAs/InGaAs double-gate (DG) and standard high-electron-mobility transistors (HEMTs) is analyzed by means of an ensemble 2-D Monte Carlo simulator. The DG-HEMT is found to have a better noise behavior than the single-gate (SG) device. The results show a moderate decrease of the P and R noise parameters for the DG HEMT with respect to that of the SG device, since current fluctuations due to electrons injected into the buffer are eliminated. Moreover, the DG HEMT reveals a significantly lower extrinsic minimum noise figure $\mathrm{NF_{min}}$ and a higher associated gain G_{ass}, not only due to the better intrinsic performance but also to the lower contact resistances.**

***Index Terms*—Double-gate high-electron-mobility transistor (DG-HEMT), Monte Carlo (MC) simulations, noise behavior.**

I. Introduction

TO FURTHER improve the high-frequency low-noise behavior of InAlAs/InGaAs high-electron-mobility transistors (HEMTs), double-gate (DG) devices have been recently developed [1]–[3]. The DG geometry (a gate is placed on each side of the conducting channel) offers numerous advantages over conventional single-gate (SG) devices, such as counteracting the effect of carrier injection into the buffer, since no buffer is used in the structure, and providing a better charge control. Thus, the DG device exhibits a better pinch-off behavior, lower output conductance g_d, and a higher transconductance g_m. Moreover, the lower resistance of the gate contact R_g leads to a considerably improved extrinsic dynamic behavior (in terms of $f_{\max}$). The source and drain parasitic resistances, R_s and R_d, respectively, are also lower due to the higher electron concentration. Due to all these advances introduced by the DG architecture, an improvement of the intrinsic and extrinsic noise performance is also expected. To clarify this point, in this brief, we perform a full theoretical study of the noise behavior of an $\mathrm{In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As}$ 100-nm-gate DG HEMT by comparing it with the corresponding standard SG structure. We make use of a semiclassical 2-D ensemble Monte Carlo (MC) simulator [4], [5], which can reproduce the static and dynamic behavior of the fabricated DG transistors [6] and has proved to be a very helpful tool in the analysis of noise behavior in devices in which an accurate description of the microscopic dynamics of carriers is essential. The intrinsic noise performance is studied in terms of the P, R, and C parameters [7] and the extrinsic one in terms of the minimum noise figure $\mathrm{NF_{min}}$, the noise resistance R_n, and the associated gain G_{ass} [8].

This brief is organized as follows. In Section II, the MC model employed in the analysis is described. Next, the main results of this brief are presented in Section III. Finally, in Section IV, the most important conclusions are drawn.

II. MC Model

For the calculations, we make use of a semiclassical ensemble MC simulator self-consistently coupled with a 2-D Poisson solver, whose validity has been checked for conventional SG [4], [5] and DG HEMTs [6]. The devices under analysis are a recessed 100-nm gate $\mathrm{In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As}$ DG HEMT and the corresponding standard SG HEMT. The detailed topology is shown in Fig. 1. The width of the devices W is 100 μm, and the layer structure is similar to that of the fabricated transistors. The SG HEMT consists of an InP substrate (not simulated), a 200-nm $\mathrm{In_{0.52}Al_{0.48}As}$ buffer followed by a 20-nm-thick $\mathrm{In_{0.53}Ga_{0.47}As}$ channel, three layers of $\mathrm{In_{0.52}Al_{0.48}As}$ (a 5-nm spacer, a 5×10^{12}-$\mathrm{cm^{-2}}$ δ-doped layer modeled as a 5-nm layer doped at 10^{19} $\mathrm{cm^{-3}}$, and a 12-nm Schottky layer), and, finally, a 10-nm-thick $\mathrm{In_{0.53}Ga_{0.47}As}$ cap layer (doped 6×10^{18} $\mathrm{cm^{-3}}$). In the DG HEMT, the buffer is suppressed and substituted by a layer structure symmetrical to that at the top of the channel.

Previously to the noise characterization of the devices, the dynamic performance must be determined. The procedure [4]–[6], [9] is the same for both types of devices, which is correct as long as the DG HEMT works in common mode, i.e., being identical the potential applied at both gate electrodes ($V_{\mathrm{GS1}} = V_{\mathrm{GS2}} = V_{\mathrm{GS}}$). Once calculated the Y parameters, the intrinsic P, R, and C noise parameters [7] are evaluated. They represent the drain and the gate current noise and their cross correlation, respectively. Then, the extrinsic minimum noise figure $\mathrm{NF_{min}}$ [8], which indicates the noise added by the device to the signal that is amplifying, and

Manuscript received December 5, 2007; revised March 7, 2008. This work was supported in part by the Dirección General de Investigación (MEC, Spain) and FEDER under Project TEC2007-61259/MIC, by the Consejería de Educación of the Junta de Castilla y León (Spain) under Project SA044A05, and by MEC under the Program José Castillejo. The review of this brief was arranged by Editor M. J. Deen.

B. G. Vasallo, T. González, D. Pardo, and J. Mateos are with the Departamento de Física Aplicada, Universidad de Salamanca, 37008 Salamanca, Spain (e-mail: bgvasallo@usal.es).

N. Wichmann, S. Bollaert, Y. Roelens, and A. Cappy are with the Département Hyperfréquences et Semiconducteurs, Institut d'Electronique, de Microélectronique et de Nanotechnologies, University of Lille, 59652 Villeneuve d'Ascq Cedex, France.

Color versions of one or more of the figures in this brief are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2008.921982

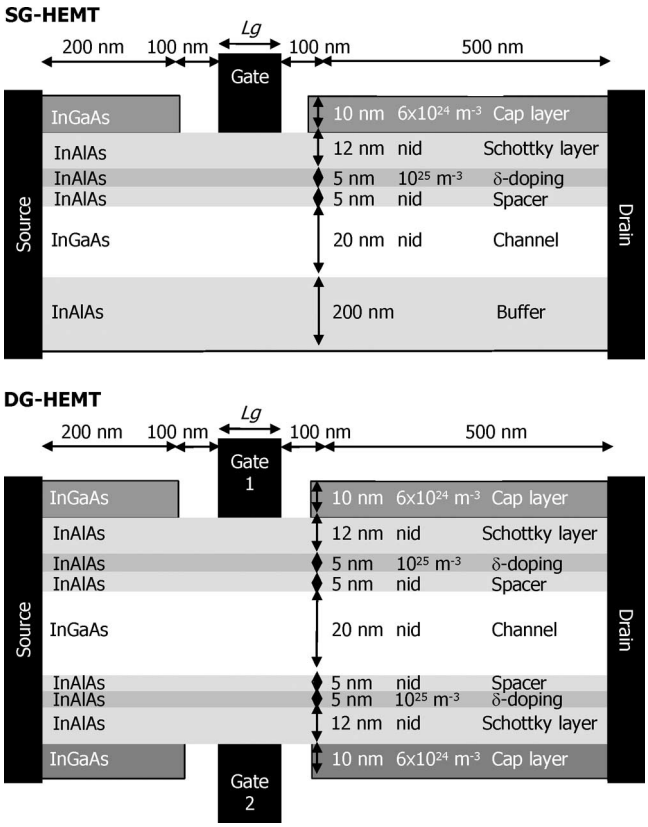


Fig. 1. Schematic drawing of the simulated SG and DG HEMTs. $L_g = 100$ nm.

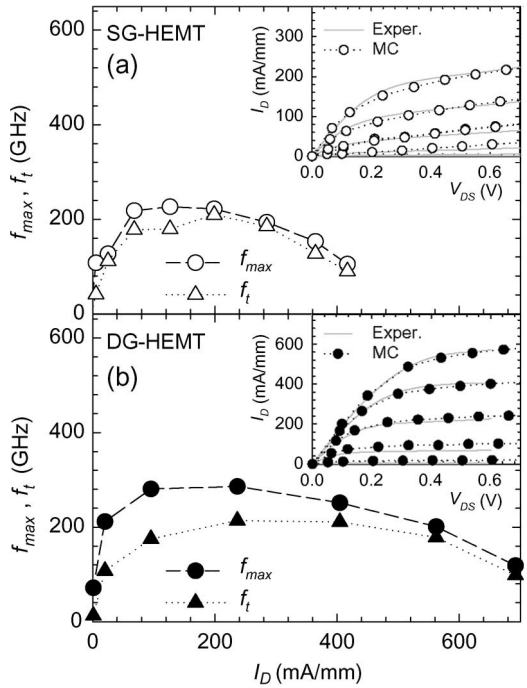


Fig. 2. MC values of $f_{\max}$ and f_t versus I_D for the (a) SG and (b) DG HEMTs. $V_{\rm DS} = 0.5$ V. Inset: Experimental and MC extrinsic output characteristics, where the gate voltage of the top curves is $V_{\rm GS} = 0.0$ V and the step of the gate bias is $\Delta V_{\rm GS} = 0.1$ V for both sets of curves.

the associated gain $G_{\rm ass}$ are evaluated by taking into account both intrinsic and extrinsic noise sources. Another important parameter to be calculated (having a key influence for circuit design) is the noise resistance R_n, which is a measure of the sensibility of $\rm NF_{min}$ to the changes of the input admittance with respect to its optimum value [8].

III. Results

To better understand their noise performances, we have previously analyzed the static and dynamic behavior of both SG and DG HEMTs [6]. The insets of Fig. 2 show the comparison between the experimental and MC extrinsic output characteristics of both devices. The drain–current I_D provided by the DG HEMT is about twice that given by the SG transistor, since the electron concentration in the DG-HEMT channel is significantly higher due to the presence of two charge-accumulation regions. Regarding the dynamic behavior, we show the extrinsic cutoff frequencies $f_{\max}$ and f_t as main parameters. The MC values of $f_{\max}$ and f_t as a function of the drain–current are shown in Fig. 2 for both 100-nm-gate SG [Fig. 2(a)] and DG [Fig. 2(b)] HEMTs with 100-μm gate width. The values taken by $f_{\max}$ are higher in the DG HEMT than in the SG structure. Particularly, the maximum values of $f_{\max}$ are 286 GHz for the DG HEMT and 226 GHz for the SG HEMT, in good agreement with the results of the measurements 288 and 220 GHz, respectively [2]. The simulations and the experiments show similar values for f_t for both devices, around 200 GHz (the intrinsic cutoff frequency f_c is also similar, since the increase of g_m in the DG HEMT is compensated by its higher gate capacitances). The improvement of $f_{\max}$ in the DG device is higher than that of f_t, due to the reduced values of R_g and g_d, which have a significant influence on $f_{\max}$ without much affecting the value of f_t. These results have already been widely explained in [6].

Concerning the intrinsic noise behavior, in Fig. 3, the intrinsic P [Fig. 3(a)], R [Fig. 3(b)], and C [Fig. 3(c)] noise parameters are shown as a function of I_D for the simulated DG and SG HEMTs, where $V_{\rm DS} = 0.5$ V. For a better understanding of the figure, since the MC results for R and C are not very accurate due to the uncertainty in the calculation of the gate noise [5] (and also the value of P for very low I_D, when g_m is practically zero), their respective tendency lines have been drawn. Moreover, it must be pointed out that the gate leakage current and its consequent shot noise, that may affect the value of R (mainly near pinch-off), are not included in our model. P and R, representing, respectively, the noise due to the drain and gate current fluctuations, take lower values in the DG HEMT than in the SG device. This happens because carriers in the DG device are completely confined in the channel, and the current fluctuations due to electrons injected into the buffer are avoided. The change between low/high horizontal velocity of electrons in the buffer/channel leads to drain–current fluctuations, while the associated vertical motion generates an excess of gate current noise. Thus, the suppression of these real space-transfer processes reduces both drain and gate current noise. On the other hand, C is about the same for both types of devices, since the electron dynamics inside the channel and the gate-channel coupling are similar.

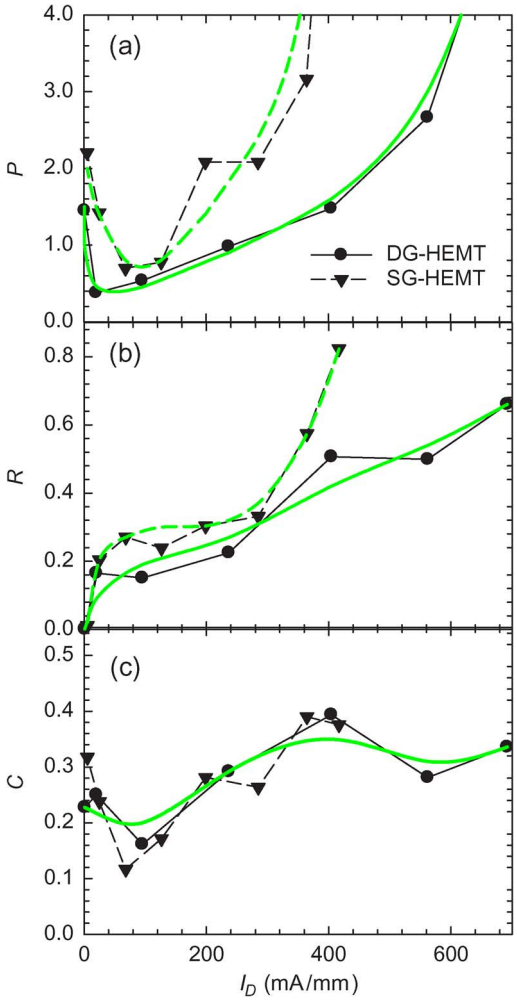


Fig. 3. MC values of (a) P, (b) R, and (c) C parameters versus I_D for the 100-nm-gate DG and SG HEMTs. $V_{\rm DS} = 0.5$ V. Their corresponding tendency lines are also plotted.

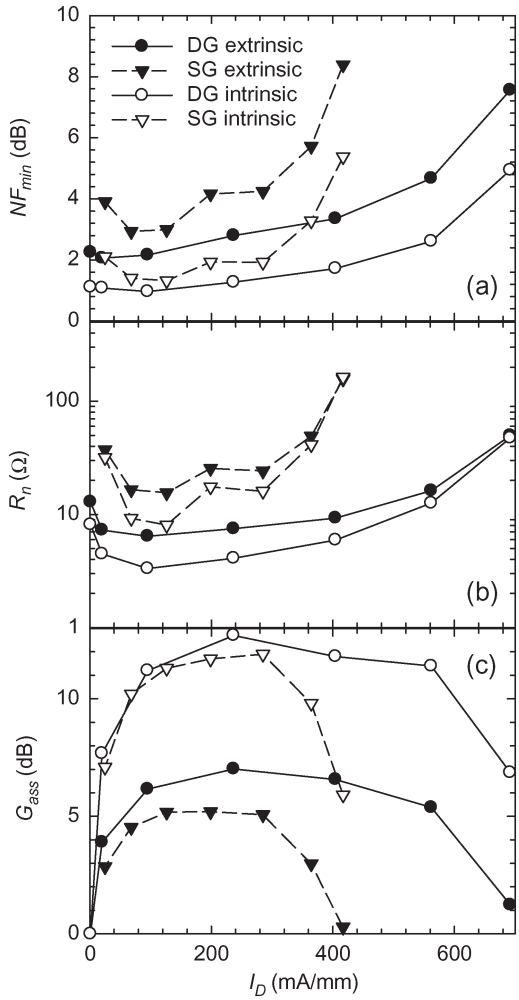


Fig. 4. Intrinsic and extrinsic MC values of the (a) $\rm NF_{min}$, (b) R_n, and (c) $G_{\rm ass}$ versus I_D for the 100-nm-gate DG and SG HEMTs at 94 GHz. $V_{\rm DS} = 0.5$ V.

The extrinsic noise performance of the devices is described through the parameters $\rm NF_{min}$ and R_n, together with $G_{\rm ass}$. In Fig. 4, we show their MC values at 94 GHz for $V_{\rm DS} = 0.5$ V as a function of I_D for both DG and SG HEMTs. The corresponding intrinsic values, calculated without considering the parasitic contact resistances R_s, R_d, and R_g, are also plotted for comparison. The minimum noise figure shows the typical U-shape, mainly due to the influence of R_n, which increases at both high (due to the increase of the drain noise, associated with the P parameter) and low (due to the decrease of the cutoff frequency) drain–current. The intrinsic $\rm NF_{min}$ is lower in the DG than in the SG HEMT (the minimum values are 1.1 and 1.4 dB, respectively) due to the reduction of the intrinsic drain and gate noise (lower P and R). When the contact resistances are taken into account, the minimum values taken by $\rm NF_{min}$ are 2.1 dB (for $I_D = 21$ mA/mm) for the DG HEMT and 2.9 dB (for $I_D = 68$ mA/mm) for the SG device. Therefore, the extrinsic $\rm NF_{min}$ is significantly improved by the use of the DG architecture, due to the better intrinsic behavior and the lower parasitic contact resistances. The extrinsic R_n and $G_{\rm ass}$ are also much improved in the DG structure, thus allowing both for a better noise matching and a higher gain at low-noise conditions and, as a consequence, a more flexible monolithic microwave integrated-circuit design.

Fig. 5 shows the frequency dependence of $\rm NF_{min}$ and $G_{\rm ass}$ for both HEMTs at the I_D providing the minimum of $\rm NF_{min}$. At these particular values of I_D, the best values of $\rm NF_{min}$ involve similar values of $G_{\rm ass}$ for both devices. The intrinsic values and those obtained considering only R_s and R_d (and not R_g) in the calculations are shown in Fig. 5. In all cases, the well-known increase of $\rm NF_{min}$ and decrease of $G_{\rm ass}$ with frequency is clearly observed. Moreover, in both types of devices, for this particular value of gate width $W = 100$ μm, the increase of $\rm NF_{min}$ due to R_s and R_d is larger as compared to that coming from the presence of R_g. However, the contribution of the different contact resistances to the extrinsic value of $\rm NF_{min}$ depends on the value of W, since R_g is proportional to W, while R_s and R_d are proportional to $1/W$. In Fig. 6, we show the values of $\rm NF_{min}$ [Fig. 6(a)], R_n [Fig. 6(b)], and $G_{\rm ass}$ [Fig. 6(a)] as a function of W at 94 GHz for both simulated DG and SG devices. For these calculations, we have supposed that the extrinsic capacitances are proportional to W, which is a good approximation only for large W.

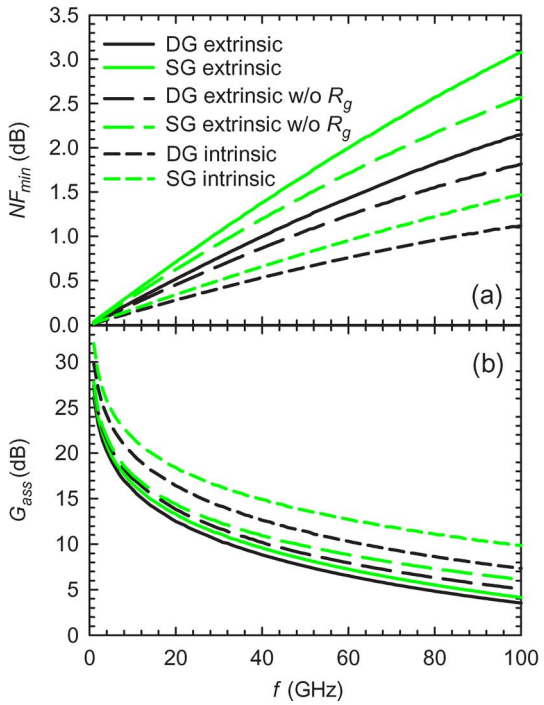


Fig. 5. Intrinsic and extrinsic MC values of (a) $\mathrm{NF_{min}}$ and (b) G_{ass} and versus frequency for the 100-nm-gate DG and SG HEMTs with $W = 100$ μm for the bias point providing the minimum of $\mathrm{NF_{min}}$ (at $V_{\mathrm{DS}} = 0.5$ V). In addition, the values calculated only considering R_s and R_d (and not R_g, labeled as extrinsic without R_g) are plotted for comparison.

Indeed, for very short W, the capacitances reach a certain saturation value, which leads to a deterioration of $\mathrm{NF_{min}}$ and G_{ass} [5], [10]. Nevertheless, these offset capacitances do not alter the comparison between the behavior of the SG and the DG HEMT, since this effect equally affects both devices. Notably, the difference between the intrinsic values of $\mathrm{NF_{min}}$ at 94 GHz for the DG and the SG devices, 0.3 dB, is increased to 0.7 dB when R_s and R_d are considered in the calculations (since their values in the DG HEMT are lower). In both cases, the values of $\mathrm{NF_{min}}$ are independent of W, as expected from the identical proportionality to $1/W$ of the contributions to the total noise of the intrinsic device and the R_s and R_d parasitic resistances. On the other hand, when all the contact resistances are taken into account, the values of $\mathrm{NF_{min}}$ increase when increasing W (with a decrease of G_{ass}), since R_g is proportional to W. Moreover, as a result of the lower R_g of the DG HEMT, the difference of $\mathrm{NF_{min}}$ with respect to the SG device increases with W, where, for example, 0.75 dB for $W = 50$ μm, 0.9 dB for $W = 100$ μm, and 1.4 dB for 200 μm (0.7 dB is coming from the difference in the intrinsic noise and the values of R_s and R_d). As a consequence, since small values of W are used for high-frequency low-noise applications, the smaller values of R_s and R_d of the DG with respect to the SG devices are much more important than those of R_g for the achievement of better noise performances. The same dependences are observed for G_{ass} [Fig. 6(c)] but taking similar extrinsic values for both devices. Finally, the intrinsic and extrinsic values of R_n [Fig. 6(b)] increase when decreasing W, but less significantly in the DG HEMT, thus providing an easier noise matching for lower W,

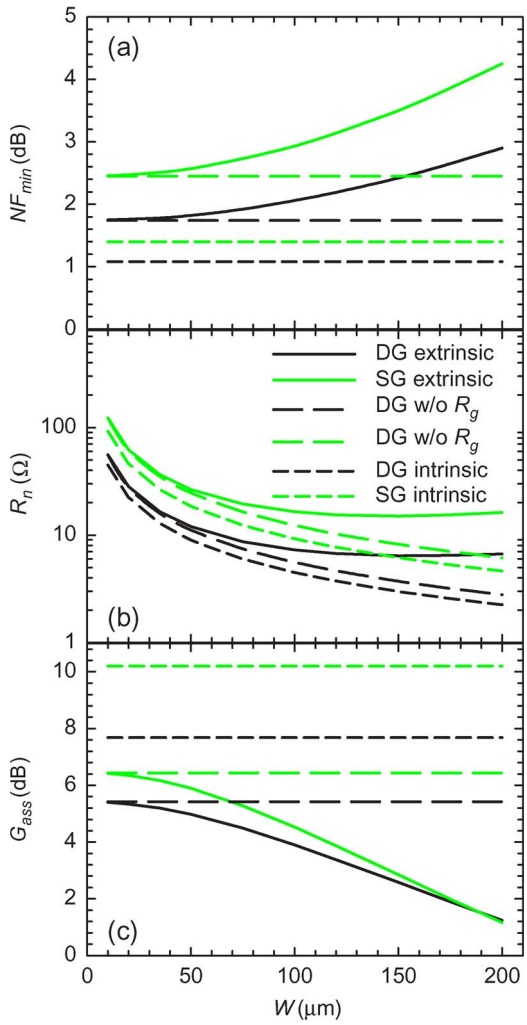


Fig. 6. Intrinsic and extrinsic MC values of (a) $\mathrm{NF_{min}}$, (b) R_n, and (c) G_{ass} versus gate width W for the 100-nm-gate DG and SG HEMTs at 94 GHz for the bias point providing the minimum of $\mathrm{NF_{min}}$ (at $V_{\mathrm{DS}} = 0.5$ V). In addition, the values calculated only considering R_s and R_d (and not R_g, labeled as extrinsic without R_g) are plotted for comparison.

which eases the circuit design for high-frequency low-noise applications.

IV. Conclusion

We have presented an MC-based study of DG HEMTs comparing the noise performance with standard SG devices. The results of our simulations show that the intrinsic P and R noise parameters in the DG are lower than in SG HEMT due to the suppression of the current fluctuations originated by the injection of electrons into the buffer. Furthermore, the extrinsic noise behavior (in terms of $\mathrm{NF_{min}}$, G_{ass}, and R_n) is significantly improved due not only to the better intrinsic noise performance but also to the lower R_s, R_d, and R_g (the latter being increasingly important for larger W).

Acknowledgment

This brief has been performed in the framework of IRCICA. The authors would like to thank Prof. F. Danneville for the helpful discussions.

REFERENCES

[1] N. Wichmann, I. Duszynski, X. Wallart, S. Bollaert, and A. Cappy, "InAlAs–InGaAs Double-Gate HEMTs on transferred substrate," *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 354–356, Jun. 2004.

[2] N. Wichmann, I. Duszynski, S. Bollaert, J. Mateos, X. Wallart, and A. Cappy, "100 nm InAlAs/InGaAs Double-Gate HEMT using transferred substrate," in *IEDM Tech Dig*., Dec. 2004, pp. 1023–1026.

[3] N. Wichmann, I. Duszynski, X. Wallart, S. Bollaert, and A. Cappy, "Fabrication and characterization of 100-nm $In_{0.53}Al_{0.47}As-In_{0.52}Ga_{0.48}As$ Double-Gate HEMTs with two separate gate controls," *IEEE Electron Device Lett.*, vol. 26, no. 9, pp. 601–603, Sep. 2005.

[4] J. Mateos, T. González, D. Pardo, V. Hoël, H. Happy, and A. Cappy, "Improved Monte Carlo algorithm for the simulation of δ-doped AlInAs/GaInAs HEMTs," *IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 250–253, Jan. 2000.

[5] J. Mateos, T. González, D. Pardo, V. Hoël, and A. Cappy, "Monte Carlo simulator for the design optimization of low-noise HEMTs," *IEEE Trans. Electron Devices*, vol. 47, no. 10, pp. 1950–1956, Oct. 2000.

[6] B. G. Vasallo, T. González, D. Pardo, J. Mateos, N. Wichmann, S. Bollaert, Y. Roelens, and A. Cappy, "Comparison between the dynamic performance of double- and single-gate AlInAs/InGaAs HEMTs," *IEEE Trans. Electron Devices*, vol. 54, no. 11, pp. 2815–2822, Nov. 2007.

[7] R. A. Pucel, H. A. Haus, and H. A. Statz, "Signal and noise properties of gallium arsenide microwave field effect transistors," *Adv. Electron. Electron Phys.*, vol. 38, pp. 195–265, 1975.

[8] H. Rothe and W. Dahlke, "Theory of noisy fourpoles," *Proc. IRE*, vol. 44, no. 6, pp. 811–818, Jun. 1956.

[9] T. González and D. Pardo, "Monte Carlo determination for the intrinsic small signal equivalent circuit of MESFETs," *IEEE Trans. Electron Devices*, vol. 42, no. 4, pp. 605–611, Apr. 1995.

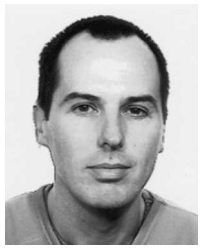
[10] B. H. Klepser, C. Bergamaschi, M. Schefer, C. G. Diskus, W. Patrick, and W. Bächtold, "Analytical bias dependence noise model for InP HEMTs," *IEEE Trans. Electron Devices*, vol. 42, no. 11, pp. 1882–1889, Nov. 1995.

Beatriz G. Vasallo was born in Salamanca, Spain, in 1978. She received the B.S. and Ph.D. degrees in physics from the Universidad de Salamanca, Salamanca, in 2000 and 2005, respectively.

She was with the Institut d'Electronique, de Microélectronique et de Nanotechnologies, France. She is currently an Assistant Professor with the Departamento de Física Aplicada, Universidad de Salamanca. Her current research interest includes the modeling and optimization of the high-frequency and low-noise performance of advanced high-electron-mobility transistors.

Nicolas Wichmann was born in Valenciennes, France, on January 5, 1979. He received the Ph.D. degree from the Institut d'Electronique, de Microélectronique et de Nanotechnologie, University of Lille, Villeneuve d'Ascq, France, in 2005, for his work on the design, fabrication, and characterization of double-gate high-electron-mobility transistors using InAlAs–InGaAs materials.

He is currently an Associate Professor with the Département Hyperfréquences et Semiconducteurs, Institut d'Electronique, de Microélectronique et de Nanotechnologies, University of Lille. His main research is focused on the design and the process development of novel nanoscaled devices for ultrahigh-speed-frequency application. He is currently involved in the realization and the characterization of III–V compounds velocity modulation transistor.

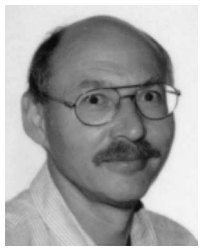


Sylvain Bollaert was born in Calais, France, on February 17, 1965. He received the Ph.D. degree from the University of Lille, Villeneuve d'Ascq, France, in 1994.

He is an Associate Professor with the Département Hyperfréquences et Semiconducteurs, Institut d'Electronique, de Microélectronique et de Nanotechnologies, University of Lille. His main research interest includes the fabrication of nanoscaled devices and monolithic microwave integrated circuits (MMICs). For the last three years, he developed the fabrication process for the 50-nm-gate-length high-electron-mobility transistors (HEMTs) using InAlAs/InGaAs lattice-matched and pseudomorphic on InP and metamorphic on GaAs. He is currently involved in the realization of ultrahigh-speed MMICs using such devices and in the development of sub-50-nm-gate-length HEMTs. His other research work is the study and the realization of ballistic devices, such as transferred-substrate HEMTs for terahertz-frequency applications.

Yannick Roelens was born in Villeneuve d'Ascq, France, on May 3, 1972. He received the Ph.D. degree from the University of Lille, Villeneuve d'Ascq, in 2000, with a dissertation on application of high-critical temperature superconductors in microwave.

Since September 2001, he has been an Associate Professor with the Département Hyperfréquences et Semiconducteurs, Institut d'Electronique, de Microélectronique et de Nanotechnologies, University of Lille. His main research interest includes the fabrication of nanoscaled devices and microwave circuits. He is involved in the realization and characterization of ballistic devices.



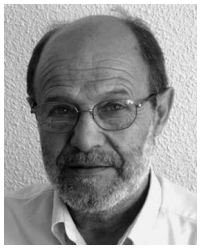
Alain Cappy (M'92–SM'96) was born in Chalons sur Marne, France, on January 25, 1954. He received the Docteur en Sciences degree from the Institut d'Electronique, de Microélectronique et de Nanotechnologies (IEMN), University of Lille, Villeneuve d'Ascq, France, in 1986, for his work on the modeling and the characterization of MESFETs and high-electron-mobility transistors.

Since 1977, he has been with the Département Hyperfréquences et Semiconducteurs, IEMN, where he is currently the Director and a Professor of electronics and electrical engineering. His main research interests include modeling, realization, and characterization of ultrahigh-speed device and circuits for applications in the centimeter- and millimeter-wave ranges.

Tomás González (M'05–SM'07) was born in Salamanca, Spain, in 1967. He received the B.S. and Ph.D. degrees in physics and from the Universidad de Salamanca, Salamanca, in 1990 and 1994, respectively.

Since 1991, he has been with the Departamento de Física Aplicada, Universidad de Salamanca, where he is currently a Full Professor of electronics. His main research activity is in the field of electronic transport in semiconductor materials and high-frequency electronic devices, with special application to the modeling of electronic noise by microscopic approaches. Recently, he is also involved in the development of novel device concepts based on ballistic transport. He is the author or coauthor of more than 100 refereed scientific journal papers and 150 conference presentations. He is member of the Editorial Board of *Fluctuation and Noise Letters* (World Scientific).

Dr. González serves on the committees of several international conferences including the International Conference on Noise and Fluctuations (ICNF), Non-Equilibrium Carrier Dynamics in Semiconductors. He was the Chairman of the 18th ICNF, held in Salamanca, in September 2005.



Daniel Pardo was born in Valladolid, Spain, in 1946. He received the B.S. and Ph.D. degrees in physics from the University of Valladolid, Valladolid, in 1971 and 1975, respectively.

From 1971 to 1981, he was with the Electronics Department, University of Valladolid, where he worked on the characterization of semiconductor materials and modeling of semiconductor devices and where he became an Associate Professor in 1978. In 1981, he joined the Departamento de Física Aplicada, Universidad de Salamanca, Salamanca, Spain, where he has been a Full Professor since 1983 and is currently the Head of the Semiconductor Devices Research Group. His current research interest includes the Monte Carlo simulation of semiconductor devices with special application to noise.

Javier Mateos was born in Salamanca, Spain, in 1970. He received the B.S. and Ph.D. degrees in physics from the University of Salamanca, Salamanca, in 1993 and 1997, respectively.

He was with the Institut d'Electronique, de Microélectronique et de Nanotechnologies. Since 1993, he has been with the Departamento de Física Aplicada, Universidad de Salamanca, where he has been an Associate Professor since 2000. His current research interest includes the development of novel device concepts using ballistic transport, together with the modeling and optimization of the high-frequency and low-noise performance of III–V high-electron-mobility transistors, including narrow and large bandgap devices based on InAs and GaN, respectively.