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# RF dynamic and noise performance of Metallic Source/Drain SOI n-MOSFETs

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ABSTRACT

This paper presents a detailed study of the RF and noise performance of n-type Schottky barrier (SB) MOSFETs with a particular focus on the influence of the Schottky barrier height (SBH) on the main dynamic and noise figures of merit. With this aim, a 2D Monte Carlo simulator including tunnelling transport across Schottky interfaces has been developed, with special care to consider quantum transmission coefficients and the influence of image charge effects at the Schottky junctions. Particular attention is paid to the microscopic transport features, including carrier mean free paths or number of scattering events along the channel for investigating the optimization of the device topology and the strategic concepts related to the noise performance of this new architecture. A more effective control of the gate electrode over drain current for low SBH (discussed in terms of internal physical quantities) is translated into an enhanced transconductance $g_m$, cut-off frequency $f_T$, and non-quasistatic dynamic parameters. The drain and gate intrinsic noise sources show a noteworthy degradation with the SBH reduction due to the increased current, influence of hot carriers and reduced number of phonon scatterings. However, the results evidence that this effect is counterbalanced by the extremely improved dynamic performance in terms of $g_m$ and $f_T$. Therefore, the deterioration of the intrinsic noise performance of the SB-MOSFET has no significant impact on high-frequency noise FoMs as $NF_{min}$, $R_n$ and $G_{ass}$ for low SBH and large gate overdrive conditions. The role of the SBH on $\Gamma_{opt}$, optimum noise reactance and susceptance has been also analyzed.



## 1. Introduction

Schottky barrier (SB) MOSFETs have a device structure similar to conventional MOSFETs in which heavily doped source and drain regions are replaced by metals or silicides to form Schottky contacts [1–3]. These devices have recently attracted a huge interest due to their remarkable features, which have situated them as potential candidates to solve some of the problems of conventional downscaled MOS transistors [4]. For example, SB-CMOS technology is fully compatible with Silicon CMOS technology, can be fabricated in a low-temperature process including high-$k$/metal-gate [5] and eliminates the need for ultra-shallow junctions and complicated channel doping steps [6]. It has been already demonstrated that CMOS circuits fabricated with SB-MOSFET technology can compete with a highly doped S/D MOSFET structure [7]. The use of silicide source and drain offers at the same time inherently reduced values of contact resistivity [4], even lower than the target values indicated in the ITRS for the year 2016 [8]. Therefore, from the point of view of the device performance, this in turn yields to a higher scalability, reduced short channel effects due to the junction abruptness [1,8], a lower sub-threshold swing [9] and high transconductance [10]. Also some authors defend the immunity of these devices to the latchup phenomena [11,12]. Thus, SB-MOSFETs appear quite attractive as promising candidates for the design of analogue applications featuring sub-100 nm nanoscaled transistor devices [3,13]. For a detailed overview and status of the SB-MOSFET technology, see [5,8,14–16].

In an accumulation mode SB-MOSFET, the injection of carriers in the channel is controlled by the metal (silicide) – semiconductor Schottky junction at the source, which is reverse biased [8]. Thus tunnelling across the potential barrier plays a crucial role to set the transition between the *on* and *off* states [1,17]. Consequently, accurate modelling of SB-MOSFETs involves the treatment of non-classical phenomena, like direct quantum tunnelling across the Schottky barrier. However, the potential barrier modulation induced by the gate severely compromises the use of one-dimensional diode equations to describe the injection at the source [18–21]. Furthermore, the study of the RF performance of SB-MOSFETs is a major issue to find out the possibilities of metal S/D MOS devices to replace doped S/D transistors in the short and mid terms [9,17,22–24]. Within this context, the high frequency noise performance of SB-MOSFETs needs to be elucidated.

In this work we have developed a two-dimensional Monte Carlo (MC) device simulator to study the influence of the main topology parameter of this architecture (the Schottky barrier height, SBH) on

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the high-frequency *ac* and noise properties of SB-MOSFETs, including the most relevant figures of merit (FoMs). It must be noticed that the stochastic nature of the Monte Carlo approach mimics the real, noisy movement of carriers inside the device [25,26] in a microscopic fashion. These features make this method to be particularly well suited for the study of submicrometric devices, since far-from-equilibrium phenomena, non-stationary and ballistic transport, short channel effects, intrinsic noise sources, etc. are intrinsically included [27]. Moreover, an exhaustive analysis of the electronic transport in SB-MOSFET devices is also carried out, including the investigation of the microscopic features of the carrier movement (transit times, mean free paths, local densities of scattering mechanisms, etc.) [27]. The procedure involves tracking any particular electron movement to obtain a recording of the characteristic transport parameters (time of free flights, scattering undergone, etc.) of the ensemble of carriers along the channel. This type of information, closely related to the microscopic transport of the carrier ensemble, is usually not accessible by other types of simulators, including commercial ones. The connection of such microscopic quantities to the intrinsic noise sources and the dynamic and noise figures of merit has not been performed up to date on a Metallic Source/Drain MOSFET.

The paper is organized as follows. Section 2 presents the topology of the devices under study, together with the main characteristics of the model developed and its implementation in the 2D MC simulator. In Section 3 the small-signal performance of the device is presented, while the high-frequency noise is discussed in Section 4, with particular attention to the influence of the Schottky barrier height (SBH) on the noise figures of merit. Finally, the main conclusions of our work are presented.

## 2. Simulated structure and Monte Carlo approach

### 2.1. Monte Carlo approach

Injection phenomena in Schottky source and drain contacts of an SB-MOSFET are mainly related to quantum effects. This means that in order to determine the charge to be injected, transmission coefficient (*TC*) must be calculated along the path perpendicular to the Schottky contacts. However, solving in a self-consistent manner the potential profiles provided by the solution of Poisson's equation and the transmission coefficients achieved by the solution of Schrödinger's equation is a rather complicated task. As a consequence, Monte Carlo simulations related to this technology have been scarcely reported (e.g. the work by Winstead and Ravaioli [21], Xia et al. [23] and the publications from the group of the Peking University [20,28]). For this purpose, we have exhaustively improved our in-house 2D Monte Carlo device simulator to be able to model in an appropriate way the physics of SB-MOSFETs and the electronic transport across the Schottky interfaces. We solve Schrödinger's equation by means of the Wenzel–Kramers–Brillouin (WKB) approach [29] which determines the *TC* along the whole silicide/silicon surfaces including in a self-consistent manner the image charge effects responsible for the Schottky Barrier Lowering (SBL). The effect of the Schottky Barrier Lowering is incorporated internally by considering it in the potential profile for the calculation of the quantum transmission coefficient, as pointed out by Winstead and Ravaioli [21]. Even though the solution of the WKB approach can present some inaccuracies for sharp barriers, careful tuning of the WKB model parameters allows obtaining similar current values to those obtained by calculating the transmission coefficient by means of more exact solutions of Schrödinger's equation as the Airy Transfer Matrix method [30]. Our model has been exhaustively calibrated to properly reproduce experimental data of Schottky barriers under the most unfavourable conditions of high inverse polarization in Schottky diodes [31] and back-to-back Schottky diodes [32] for a wide temperature range and several values of the SBH. The procedure that accounts for thermionic and tunnel injection/absorption mechanisms has been carefully developed for the two-dimensional case. It is worth to mention that thermionic and quantum tunnelling currents are calculated by accounting the number of particles crossing the Schottky barrier in both senses, injection and absorption components (and not by analytical or numerical calculations for the current at the contact). The Schottky barrier interface is considered to be ideal in the simulations. Since effects such as interface traps or dipole fluctuations must play a role mainly in the low-frequency regime, this shall not significantly modify the conclusions presented in this paper. As our approach is fully two-dimensional, not only the SBL but also the potential energy profile is different at each vertical position of the mesh, yielding to different local quantum transmission coefficients. The 2D thermionic-and-tunnel-injection/absorption procedure is detailed in [33], in which the physical principles of operation of SB-MOSFETs (with a constant barrier height of 0.20 eV) have been studied as well as the transition of the device from triode to saturation regime by means of the study of internal quantities such as the potential, carrier density or average carrier velocity.

We solve Poisson's equation each 1 *fs*. The mesh size in the channel or in the buried oxide is consistently fitted to consider the characteristic shape of the electron concentration. The number of simulated particles is around 50,000, and may vary depending on the bias point. The main aspects of our two dimensional MC simulator (band structure, scattering mechanisms, etc.) can be found in [26,27]. The longitudinal profiles along the channel of the different internal quantities (carrier concentration or velocity, etc.) are obtained properly weighting each 2D quantity over the channel by the local concentration along the vertical axis [27]. In this work we show different quantities related to the stochastic movement of the electron in the channel (as the average transit time across the channel, or mean free path between scatterings) that are provided by our Monte Carlo simulator following the procedure detailed in [27]. In parallel, we will describe also the high-frequency performance in the RF and microwaves frequency domain [34], thanks to our all-in-one modelling tool which is particularly adequate for investigating the optimization of the SB-MOSFET topology.

The use of silicides with low SB heights together with dopant-segregation (DS) layer close to the Schottky contact in the SB-MOSFET transistor is a promising solution to lower the effective SB of the structures [20,22,32,35]. This causes a substantial increase of the drain current that has been measured experimentally [5,35,36] and also observed by means of simulations of transistors and back-to-back diodes [22,32,35,37]. Important efforts are being devoted in the last few years to the DS Schottky junction engineering [15,16]. This leads to several technological possibilities, with different features of the DS layer, to finally achieve a given low effective SBH [32,38], which is the parameter considered in this work.

### 2.2. Simulated structure

The simulated structure consists of an n-channel accumulation-mode SB-MOSFET on SOI substrate presented in Fig. 1. As we can observe, the topology is similar to that of a conventional SOI-MOSFET, but the source and drain doped regions have been replaced by Schottky junctions. A differential factor of the SB-MOSFET architecture which can be also noticed in the figure is the *underlap* length, $L_{un}$, (instead of the overlap region of conventional MOSFETs). The main characteristics of the device (geometry, channel doping, etc.) are detailed in Table 1 and were chosen following the SB

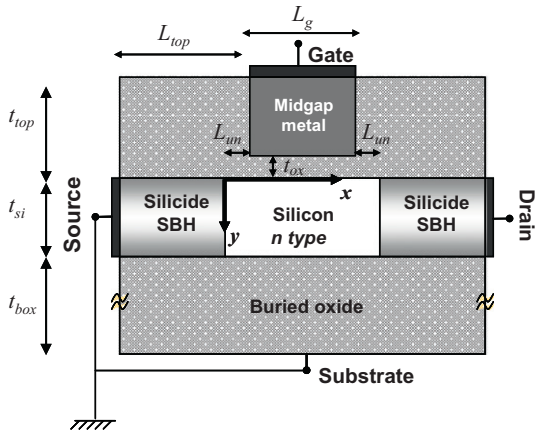


**Fig. 1.** Schematic of the simulated SB-MOSFET.

**Table 1**
Main parameters considered in the simulated structures.

| Parameters | Value | Description |
|---|---|---|
| $L_g$ | 120 nm | Gate length |
| $L_{un}$ | 5 nm | Underlap length |
| $t_{si}$ | 10 nm | Body thickness |
| $N_{Dsi}$ | $2 \times 10^{15}$ cm$^{-3}$ | Channel doping |
| SBH | 0.15–0.25 eV/tuned | Schottky barrier height |
| $t_{top}$ | 50 nm | Top oxide thickness |
| $L_{top}$ | 50 nm | Top oxide length |
| $t_{ox}$ | 2.2 nm | Gate oxide thickness |
| $t_{box}$ | 400 nm | Buried oxide thickness |

p-MOS structure proposed in [17]. Space-quantization effects are not included in the simulation. As pointed out in [39] an increase of the threshold voltage due to effective 2D quantization of the channel of SOI devices is expected to appear for active layer thicknesses lower than 10 nm. Regarding the phonon-limited mobility of carriers in single gate devices, Monte Carlo simulations have shown that under moderate and high effective vertical fields and with active layer thickness of 10 nm this quantity does not show a relevant deviation as compared to bulk transistors (see i.e. [40]). In the particular case of SB MOSFETs, as pointed out by Vega and Liu [41] space-quantization effects (and the subsequent carrier depletion close to the gate oxide) could play some role on the barrier shape and modify the effective barrier height. However, such space-quantization effects would be expected to be more relevant in double gate dopant-segregated devices with a very high impurity concentration, for which the carrier concentration shall appreciably rise in the areas close to the source contact.

Additionally, we have considered three different values for the barrier height SBH 0.25 eV, 0.20 eV and 0.15 eV. These values fall within a range between the minimum state-of-the art values achieved by single rare-earth silicides (0.28 eV) and the barrier heights obtained with a moderate use of the dopant segregation technique (0.16 eV) [42,43]. This seems to be adequate taking into account the topology of the simulated structures and the model considered. The aggressive use of dopant segregation (with much higher doses and energies), has permitted to achieve effective barrier heights in Schottky contacts near to 0.1 eV, taking PtSi as the starting material [44,45]. However, the role of such extremely doped layers in the dynamic and RF noise performance of n-type SB-MOSFETs is still an open question and lies beyond the scope of this paper; on the other hand, since thermal noise is expected to be the dominant noise source in the high-frequency range, an additional SBH reduction beyond the range considered here is not expected to qualitatively change the main conclusions shown in this work.

## 3. Effect of Schottky barrier height in the dynamic performance of the device

### 3.1. Static results

Prior to investigate the dynamic and high-frequency noise performance of the device and its optimization by the SBH, some static results must be analyzed. Fig. 2 a shows the transfer characteristics for $V_{DS}$ = 2.0 V. The ratio between the quantum tunnelling injection current over the total current at the source for the three values considered for the Schottky barrier height is presented in Fig. 2b. The current components shown in Fig. 2b correspond to the aggregated values of the entire (source) contact. The threshold voltage $V_T$ is strongly related to the SBH value and increases when the barrier height augments, a result in good agreement with [17,38]. We obtain 0.95 V, 0.70 V and 0.55 V for SBH 0.25 eV, 0.20 eV and 0.15 eV respectively (Fig. 2a).

Results obtained by means of the commercial Atlas/Silvaco simulator for a device with SBH equal to 0.20 eV are also depicted for comparison in Fig. 2a. Atlas simulation, although not including SBL in a full consistent way, can correctly treat this effect in a first-order approximation, thus providing suitable results from the DC standpoint and allowing the comparison between both simulators at this level (with main focus on the total current in saturation

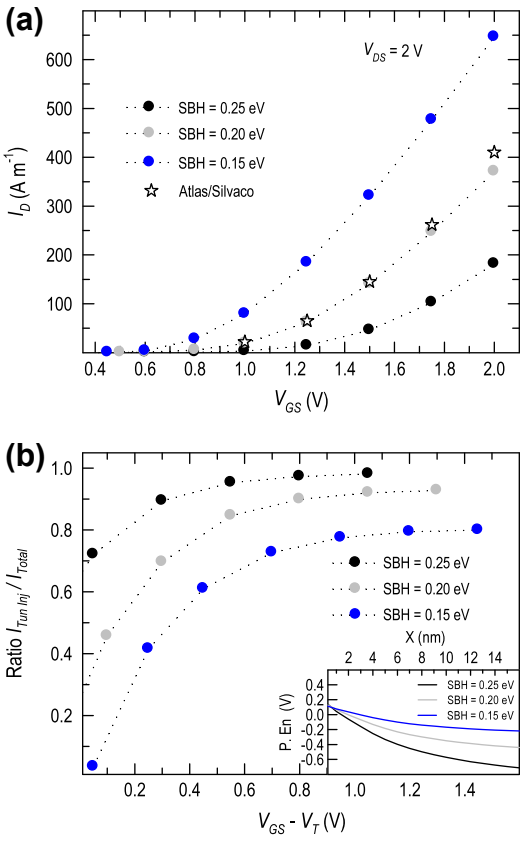


**Fig. 2.** Monte Carlo results of transfer characteristics for three values of SBH and $V_{DS}$ = 2 V (circles) (a). Stars represent the obtained $I_D$–$V_{GS}$ curves by means of the commercial Atlas/Silvaco simulator for a SBH equal to 0.20 eV. Ratio between quantum tunnelling injection current and total current (at the source terminal) for the three different values of SBH and $V_{DS}$ = 2 V (b). The inset of (b) depicts the average potential energy profile at the source vicinity for $V_{DS}$ = 2 V and $V_{GS} - V_T$ = 1.3 V.

conditions). As it can be observed, a very good agreement is found between both simulations. The results show that the variation of the barrier height is a handy way to let the *on* current to reach adequate values for most practical applications [19] and plays an important role in the injection of carriers in the channel. As it can be seen in the figure the current in the *on* state is drastically improved between the lowest and the highest SBH. Thermionic emission at the source is clearly favoured (Fig. 2b) at low SBHs as a consequence of the Schottky barrier lowering [46,47]. The values of the simulated barrier heights correspond to the zero-bias barrier values, i.e., not lowered barriers. However, when the SBH increases, the tunnelling path (the SB width) is shorter, yielding a higher probability of crossing the barrier by means of field emission, as it can be captured from the potential energy profile at the vicinity of the source (inset of Fig. 2b). This potential energy profile corresponds to the average values in the whole active region properly weighted by the electron concentration along the vertical *Y* axis, as explained in Section 2.1 and in [27]. For a fair comparison, we show the results for identical gate overdrive conditions $V_{ov} = V_{GS} - V_T = 1.3$ V.

The carrier injection through the source SB is also modulated by $V_{GS}$. In fact, as the gate overdrive increases, the barrier becomes thinner, promoting an enhanced tunnelling carrier rate [8,17]. At the same time, the higher local electric field contributes to lower the barrier height through the image force effect, thus modifying as well the thermionic component. The tunnelling current ratio at the source approaches unity for the largest barrier height and for the highest values of $V_{GS}$. It can be concluded that the gate terminal plays a key role in controlling the tunnelling current at the source by modulating the effective height and width of the SBH. An interesting feature of the transport regime deserves a special attention: due to the vertical modulation of the potential energy profile induced by the gate, most of the charge is injected just below the gate oxide, and the amount of injected charge becomes strongly reduced as one gets downwards inside the active layer. However, unlike the conventional MOSFET where the charge is highly concentrated in the inversion layer, since the channel of the SB-MOSFET is under accumulation regime, once the electrons are injected they are distributed at rather wide angles towards the channel volume [21,33]. This aspect is relevant from the standpoint of noise, as we will see afterwards. This two-dimensional effect due to the gate electrode has been also observed in double-gate SB-MOSFETs [48,49].

### 3.2. Dynamic performance of the device

Let us now focus on the extraction of the main high frequency dynamic figures of merit of the SB-MOSFET by performing a detailed small-signal analysis. In order to investigate the ac behaviour one may consider in a first step the complex frequency-dependent two-port admittance *Y* parameters. From the admittance parameters, it is possible to extract a small-signal equivalent circuit (SSEC), which is more meaningful for analysis purposes. The topology of the circuit considered (Fig. 3) as the intrinsic SSEC is the one commonly used in the literature for the study of FET devices [50]. Quasi-static versions of this SSEC have been previously considered also for SB-MOSFETs [17,23,24]. Our method allows us to determine a non-quasistatic SSEC including the channel charging resistance, $R_i$, and the propagation delay time, $\tau$, that are necessary in order to get an accurate description of the small-signal response [51–54]. From the experimental point of view, the extraction of SSEC parameters differs from that of conventional MOSFETs, since the source and drain contact resistances are bias-dependent and "cold" measurements are therefore not convenient [17]. In the present work, we have obtained the admittance parameters as a function of frequency from the Fourier analysis of the transient response of

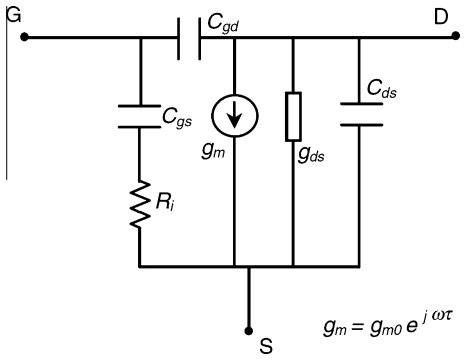


**Fig. 3.** Topology of the considered small-signal equivalent circuit.

the instant currents when adequately chosen small step voltage perturbations are applied at the terminals separately. The real and imaginary part of the four *Y* parameters versus frequency, obtained by means the procedure for Ensemble MC simulators detailed in [50,55], are shown in Fig. 4a and b – solid lines. To check the validity of the extracted parameters of the SSEC, we used them to recalculate the *Y* parameters in order to compare those with the original ones obtained from the dynamic simulation. As it can be observed in Fig. 4, an excellent overall agreement is seen between the original and the recalculated (circles) *Y*-parameters up to 100 GHz, thus demonstrating the accuracy of the non-quasi-static SSEC and the validity of the extraction procedure. From now on the results shown will correspond to the SSEC parameters for the intrinsic transistor, considering so the device structure between source and drain Schottky interfaces.

Fig. 5a and b show respectively the transconductance, $g_m$ and the cut-off frequency $f_T$, when the device is biased in the saturation regime ($V_{DS} = 2.0$ V). Some recent data for $g_m$ have been included [56,57] corresponding to conventional MOSFETs with similar

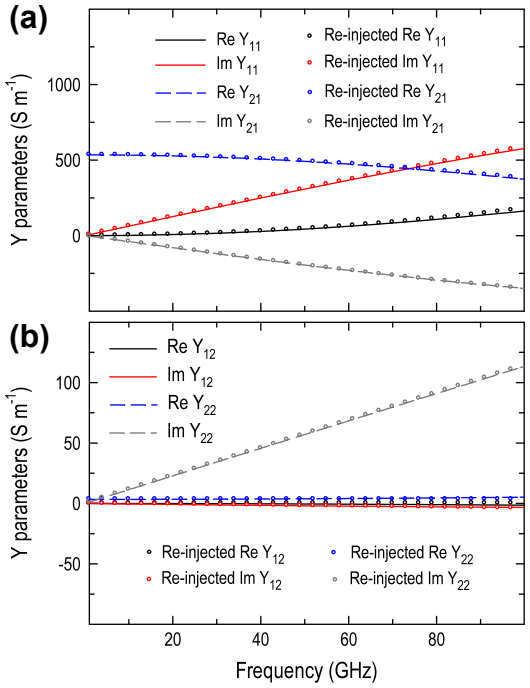


**Fig. 4.** Real and imaginary parts of the four *Y* parameters versus frequency (lines) and re-calculated *Y* parameters (circles) obtained from the extracted parameters of the SSEC shown in Fig. 3. The results correspond to the transistor with SBH equal to 0.2 eV for bias conditions of $V_{DS} = 2.0$ V and $V_{GS} = 2.0$ V.

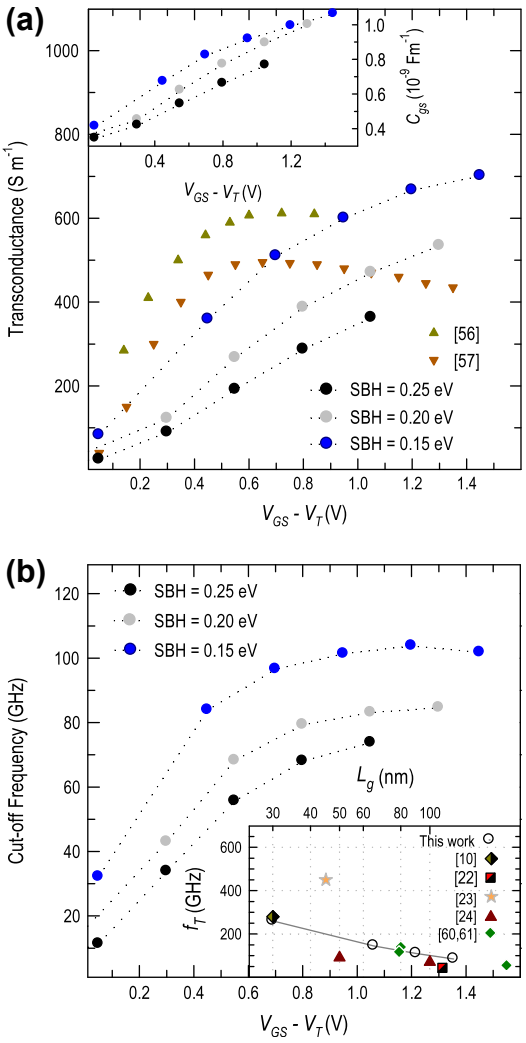


**Fig. 5.** Transconductance $g_m$ (a) and cut-off frequency (b) as a function of $V_{GS} - V_T$ for $V_{DS}$ = 2 V and SBH equal to 0.15 eV, 0.20 eV and 0.25 eV. Inset of figure (a) shows the $C_{gs}$ capacitance as a function of the gate overdrive and the three SBH values. Inset of figure (b) exhibits our Monte Carlo calculations for $f_T$ as a function of the gate length together with state-of-the-art $f_T$ for several devices [10,22–24,60,61]. Semifilled symbols correspond to SB-pMOSFETs.

characteristics for RF applications. The transconductance of the SB-MOSFET increases with the gate voltage in the saturation regime. As it can be observed in the figure, as compared to conventional MOSFET devices, the saturation of $g_m$ seems to occur at a higher $V_{GS}$, a signature of the fact that in strong saturation the carriers in the SB-MOSFETs suffer fewer scatterings at the $Si/SiO_2$ interface [55,58]. Fig. 5 corresponds to a gate bias range above that of the sub-threshold regime of the SB-MOSFET, so we did not observe the nonlinear effects that appear in the transition between purely thermionic transport (in which the carriers are injected from the source over the Schottky barrier) and the transition region, in which thermionic and field emission processes are involved [9,17]. In our case both processes account for the injection of carriers, as can be inferred from the percentage of tunnelling processes shown in Fig. 2b.

Regarding the barrier height dependence, as it can bee seen in Fig. 5a an improvement of the transconductance, $g_m$ is consistently obtained when the contact SBH is reduced, as observed in p-type transistors [17]. Moreover, the gate-to-drain, $C_{gd}$, and drain-to-source, $C_{ds}$, capacitances (not shown) of the SSEC are negligible in comparison to the gate-to-source one, $C_{gs}$, a result in good agreement with [17,23]. This quantity (related to the increase of the channel charge when a small variation in $V_{GS}$ is applied) is depicted in the inset of Fig. 5a. It is worthwhile to identify, following the procedure explained in [59], the origin of the enhanced transconductance for lower SBH. In that spirit and considering a chosen small $V_{GS}$ voltage step we have analyzed the increase of charge, $\Delta n$, increase of velocity, $\Delta v$, and the absolute value of both quantities, $n$ and $v$. Our results point out that the larger $g_m$ observed in Fig. 5a is mainly attributed to the $\Delta n \cdot v$ factor because both absolute velocity and charge variation are simultaneously enlarged in the major part of the channel when the SBH is reduced. $g_m$ reaches a maximum (in the bias range considered) of 700 S m$^{-1}$. On the other hand, the slight increase of the $C_{gs}$ capacitance when reducing the SBH is caused by the $\Delta n$ term, due to an enhanced charge injection towards the channel in the region closer to the source. In other words, the lowering of the SBH can be translated in a more efficient control of the gate electrode over the channel accumulation charge. To a lesser extent, the $g_m$ enhancement with the SBH reduction is also reflected in the unity-gain cut-off frequency $f_T$, Fig. 5b. The $f_T$ value is obtained by extrapolating the plot of the absolute value of the $Y_{21}$-to-$Y_{11}$ ratio versus frequency. The extracted values are in good agreement with the results obtained from the simplified expression $f_T \approx g_m/(2\pi(C_{gs} + C_{gd}))$ [55,60]. While the observed improvement in $g_m$ is at least around 70% when reducing the barrier height from 0.25 eV to 0.15 eV, the maximum intrinsic $f_T$ is increased just by a 41% (from 73 GHz to 103 GHz). This observation is consistent with that obtained by other authors in p-type [17] and n-type [60] SB-MOSFETs. The reason is the improved carrier injection through the SB at the source, which originates a simultaneous dependence of $g_m$ and $C_{gs}$ on the SBH, which partially compensates each other. From our results it can be concluded that the main factor responsible for the improvement of $f_T$ when SBH is reduced is the increase of the absolute velocity of carriers inside the channel. Values of $f_T$ for an n-type or p-type SB-MOSFET are scarcely reported so far and correspond to a wide spread of $L_g$ values [10,22–24,60,61]. With the aim of performing a fair comparison of our results to the ones found in the literature we have performed simulations by downscaling the SB-MOSFET from an $L_g$ value of 120 nm towards 30 nm, and the evolution of $f_T$ is depicted in the inset of Fig. 5b for a fixed value of SBH equal to 0.20 eV. The results obtained (for the 65 and 90 nm devices) are similar to the ones obtained for the Monte Carlo simulation of conventional n-MOSFET [34]. Moreover, our SB-MOSFET results are also close to others obtained in SB n-MOSFETs using SILVACO [24], or experimental [10] and simulated [22] SB p-MOSFET and are in a good accordance also to recent values obtained experimentally for a dopant segregated n-type SB-MOSFET [60,61].

The non-quasistatic parameters of the SSEC, $R_i$ and $\tau$, are essential in order to achieve a correct description of the high frequency dynamic behaviour of the devices. To the authors' knowledge they have not previously shown before for an SB-MOSFET transistor. The methodology for the extraction of $R_i$ and $\tau$ can be found in [50,55]. In the microwaves frequency range, a delay-time exists between the channel response (drain current) and the channel excitation ($V_{GS}$ variation) and it is represented by a complex transconductance in terms of the circuit elements. Some authors suggest a direct connection between $R_i$ and $\tau$, even indicating that the transconductance delay time corresponds (or it is directly proportional) to the charging time of $C_{gs}$ via $R_i$ [52,55]. Fig. 6 shows the results obtained for the intrinsic channel resistance $R_i$ and the propagation delay time $\tau$ [52] as a function of $V_{GS} - V_T$ for $V_{DS}$ = 2.0 V. The $R_i$ intrinsic charging resistance accounts for the distributed effect of the charge in the active region. In the case of conventional MOSFETs, it has been exhaustively shown that $R_i$ is practically proportional to $1/g_m$ for $V_{GS}$ in strong saturation conditions, (see e.g. [52,55]). In fact, the results of our simulation

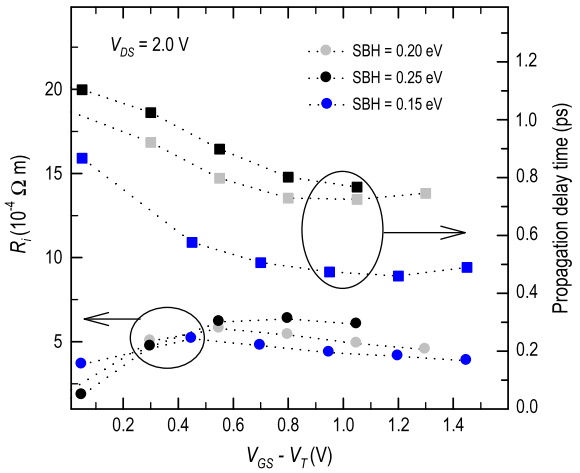


**Fig. 6.** Intrinsic channel charging resistance $R_i$ –circles – (a) and transconductance propagation delay time $\tau$ –squares – (b) as a function of the gate overdrive for the three SBH values.

indicate that also for SB MOSFETs and for ($V_{GS} - V_T > 0.4$ V), slightly lower values of $R_i$ are obtained when the SBH is reduced, actually following the opposite trend of that of the transconductance (Fig. 5a). As $V_{GS}$ is reduced and approaches the threshold voltage, the electron charge inside the channel tends to reduce for all SBH and is not so tightly controlled by the gate terminal. Consequently, as we approach to zero current conditions the values of both $g_m$ and $R_i$ tend to be closer for all the SBH considered. These observations can be otherwise attained from the transconductance propagation delay time, $\tau$. This quantity is related to the time required by the drain current to adapt to gate-to-source bias variations, typically in the order of picoseconds, and its incorporation to the model is crucial once the operating frequency falls inside the microwave range. As we can observe, $\tau$ reduces with the increase of $V_{GS}$; this can be attributed to the fact that the accumulation layer is strongly assembled to the source contact for larger values of the gate overdrive [33]. Fig. 6 reveals that the reduction of SBH and the increase of the gate overdrive (for $V_{GS} - V_T > 0.4$ V) of an SB-MOSFET have a direct consequence in the injection mechanism and promote in practice a faster response of the charge within the channel to small-signal voltage variations at the gate at very high-frequencies. This is consistent with the principle of operation of the SB-MOSFET transistor, in which the gate overdrive is directly involved in the width of the potential barrier at the source contact, affecting the quantum transmission coefficient that controls the injections of carriers at the channel. One point of utmost interest is also that the values obtained for the propagation delay time, $\tau$, are close to the values obtained for a bulk conventional MOSFET [62] of analogous gate length. Also, it is worth noting that the values of the transconductance delay time are of the same order of magnitude that the transit time, $t_t$, of the carriers and will be shown later.

## 4. High-frequency noise and microscopic transport of the SB-nMOSFET: influence of the Schottky barrier height

To confirm the suitability of SB-MOSFETs for high-frequency analogue applications it is necessary to analyze the impact of the SBH on the noise performance of the transistors. Starting from the main sources of internal noise supplied by our in-house Ensemble MC model (provided without introducing any pre-assumption about the noise origin), our purpose is to connect the internal microscopic transport mechanisms that control the transport in the devices with the main noise figures of merit, with particular interest in the minimum noise figure, $NF_{min}$. The Fourier analysis of the instantaneous current during long-time simulations (over 1 ns) allows the calculation of the typical intrinsic noise generators which represent the noise in FET devices: the spectral density of gate ($S_{IG}$) and drain ($S_{ID}$) current fluctuations, respectively, and their cross-correlation [34]. We have checked (not shown in the graphs) that $S_{ID}$ exhibits white noise dependence for frequencies up to 100 GHz. With regard to $S_{IG}$, it shows a $f^2$ dependency. These dependencies are in good agreement with the results predicted by the general theory for FETs [63] and in particular with the results previously observed in bulk MOSFETs [26,59].

In Fig. 7, the dependency with the gate overdrive of the power spectral density of gate current fluctuations $S_{IG}$ (for a frequency of 6 GHz) (a) and drain current fluctuations $S_{ID}$ (b) for the three values of SBH is shown. It can be checked that, due to the stronger control of the gate terminal, an intensified coupling to the gate of charge fluctuations in the channel (larger $S_{IG}$) exists for the lowest value of SBH, especially at high gate biasing. The values obtained for $S_{ID}$ in the Schottky-barrier MOSFET (Fig. 7b) are in the same order of magnitude that the values obtained for a fabricated FD SOI MOSFET of channel length of 160 nm [26], which are also plotted in Fig. 5b for comparison. $S_{ID}$ in conventional bulk [59], SOI MOSFETs [26], and SB-MOSFETs follows analogous variation with $V_{GS} - V_T$, which has its origin in the influence of the phenomena responsible of the excess noise generation, like hot carrier effects in the channel [64]. For all the $V_{GS}$ range considered, $S_{ID}$ increases as SBH decreases, but the difference is outstanding when $V_{GS}$ reaches the highest values. A recent study has pointed out the role of the SBH on the power spectrum current noise at low frequencies in SB-MOSFETs [65]. Although the physical mechanisms responsible for the noise are very different at low and high frequencies, in view of the results presented here and those from Ref. [65] it can be inferred that the SBH and the biasing seem to have a strong

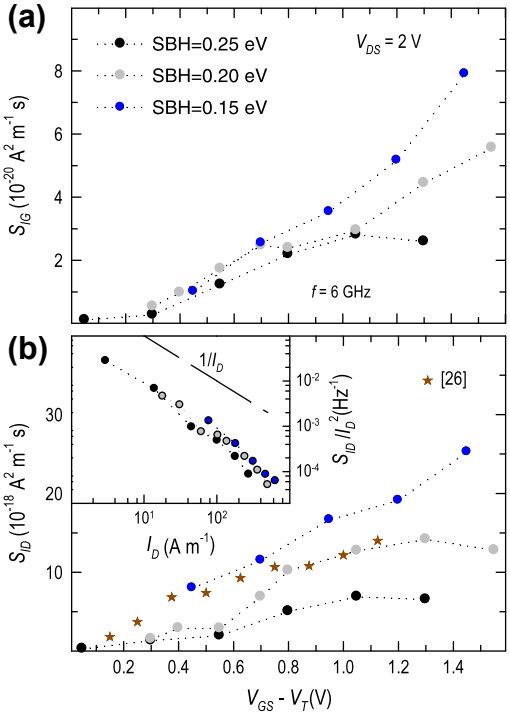


**Fig. 7.** Spectral density of gate ($S_{IG}$) at 6 GHz and drain ($S_{ID}$) current fluctuations ((a) and (b), respectively) as a function of $V_{GS} - V_T$ for $V_{DS}$ = 2 V and SBH equal to 0.15 eV, 0.20 eV and 0.25 eV. Monte Carlo $S_{ID}$ values obtained for a fabricated FD SOI MOSFET [26] are also shown for comparison (stars). Normalized drain current noise $S_{ID}/I_D^2$ as a function of $I_D$ is depicted in the inset of figure (b). Labels of figure (b) and inset of figure (b) are identical to those of figure (a).

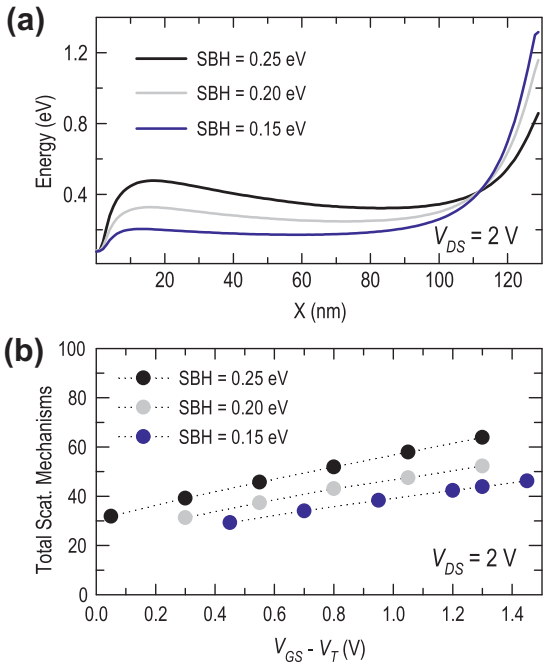


**Fig. 8.** Profile of the average carrier energy (a) at $V_{DS}$ = 2 V and $V_{GS} - V_T$ = 1.3 V for the three different values of SBH. Average values of the scattering mechanisms undergone by the carriers in the channel (b) as function of the gate overdrive for $V_{DS}$ = 2 V.

influence on the intrinsic noise results, both at low and high frequencies.

We have to bear in mind that the worsening of $S_{ID}$ with SBH is accomplished by a non negligible increase in the drain current (Fig. 2), so that if we analyze the normalized drain current noise as function of $I_D$ (inset of Fig. 7b), this behaviour finally results in just a slight degradation of $S_{ID}$ with the SBH lowering. Second, some considerations must be made about the sensitivity of $S_{ID}$ with the SBH and the features of electronic transport. To tackle this analysis, we have carried out a further inspection of the profile along the channel of internal properties simultaneously with the quantities related to the microscopic electronic transport (transit time, average travelled length, etc.).

Fig. 8a exhibits the average carrier energy profiles along the channel considering a constant applied drain bias equal to $V_{DS}$ = 2.0 V and a gate overdrive voltage equal to 1.3 V for all the structures. This is an important quantity to be analyzed due to the influence of energetic carriers on excess noise within the channel [26]. As it can be observed, in the SB-MOSFET there is a significant presence of hot carriers along the channel (particularly relevant close to the forward biased drain terminal) as a consequence of the severe increase of the electric field [33,49]. This is emphasized by the reduction of the density of phonon scattering mechanisms with the SBH drop (Fig. 8b), which are the main responsible of minimizing the correlation of drain current fluctuations by relaxing the electron momentum. For instance, for $V_{DS}$ = 2.0 V and $V_{GS} - V_T$ equal to 1.3 V, the reduction in the SBH from 0.25 to 0.15 eV diminishes the average number of phonon scatterings from 64 to 44. We must also bear in mind that the channel is maintained undoped, and under saturation conditions, the high values of carrier velocity make the carriers to strongly minimize surface interactions [21,33]. In fact, surface roughness scattering becomes negligible (about three scatterings) as compared to the more relevant isotropic phonon scattering. This behaviour evidences that the thermal noise (associated to the modulation of the resistivity of the channel, which is the primary origin of the spectral density of drain current fluctuations $S_{ID}$) is amplified with the reduction of the SBH.

On the other hand, the average longitudinal velocity is moderately enhanced with the SBH reduction (not shown in the graphs) and naturally explains the reasonable decrease of the average transit time of carriers, $t_t$, from 1.57 ps to 1.35 ps for $V_{GS} - V_T$ = 1.3 V (Fig. 9a). $t_t$ is a meaningful indicator of how rapid are the electrons travelling across the channel. It is also interesting to note that, even if the values of the velocity in most of the channel are larger than the saturation velocity of electrons in *bulk* Si, $v_{sat}$ [33], the transit time values are above the simplified approximation $L_g/v_{sat}$ (being $L_g$ equal to 120 nm). This obeys to the previously mentioned microscopic transport in the accumulation mode SB-MOSFET, which exhibits a strongly diffusive character since the free carriers spread all over the active region [21]. To verify this assertion we present in Fig. 9b the average total travelled distance, $R$ (calculated by recording the two-dimensional movement of carriers), which clearly surpasses $L_g$. This behaviour is strongly influenced by the electric field from the gate [49] and the SBH. This point is especially well exemplified for the lower SBH in which $t_t$ is closer to the previously mentioned simplified theoretical approach, indicating that the carrier movement slowly turns into more one-dimensional. Moreover, regarding the mean free path, $\lambda$, (Fig. 9b), as it can be observed it ranges from 7 to 9 nm depending on the SBH and the gate bias condition, meaning that, in average, the carriers can travel larger free paths between scatterings events as SBH is reduced, which in turn contributes to a greater influence of the thermal noise.

Taking into account the results obtained for the intrinsic noise sources (Fig. 7), one could think about a degraded noise performance if the SBH is reduced. However, we have to bear in mind that the typical circuital four noise parameters used by circuit designers (minimum noise figure $NF_{min}$, noise resistance, $R_n$, and phase and magnitude of the complex optimum reflection coefficient, $\Gamma_{opt}$) encompass the weight of $S_{ID}$, $S_{IG}$ and their cross-correlation, together with the main dynamic figures of merit. These circuital noise parameters are calculated in our case from the noise

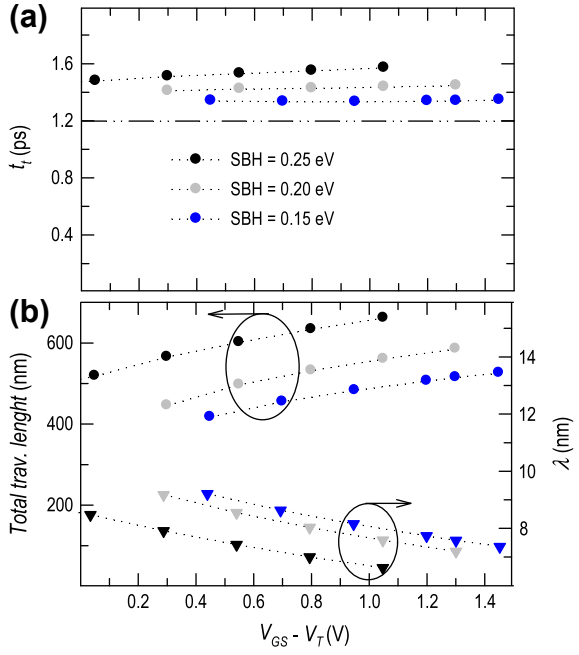


**Fig. 9.** Average values of the transit time of the carriers in the channel (a), two-dimensional total travelled length (circles) and calculated mean free path of the carriers (triangles) (b), as a function of the gate overdrive for $V_{DS}$ = 2 V and the three different values of SBH.

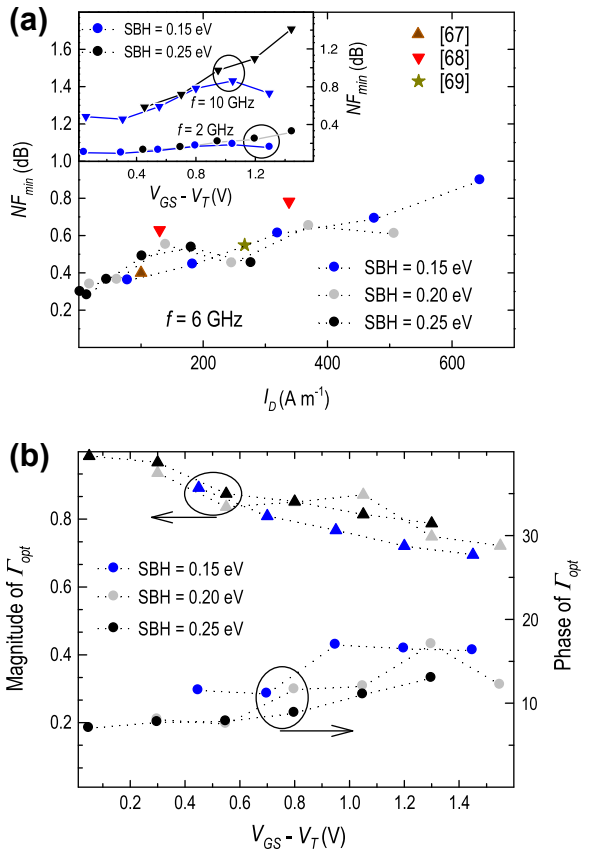


**Fig. 10.** Minimum noise figure $NF_{min}$ (a) and module and phase of $\Gamma_{opt}$ (b) versus $I_D$ for $V_{DS}$ = 2 V at 6 GHz (b) for the three different barrier heights. $NF_{min}$ data of conventional MOSFETs are included for comparison [67–69]. Inset of figure (a) depicts the $NF_{min}$ versus gate overdrive for two additional values of frequency and SBH equal to 0.15 eV and 0.25 eV. Module and phase of $\Gamma_{opt}$ (b) versus $V_{GS} - V_T$ for $V_{DS}$ = 2 V at 6 GHz for the three different barrier heights. The device width is considered to be 100 μm.

correlation matrix, as explained in [64]. In particular, the most relevant noise FoM, $NF_{min}$ (Fig. 10a), which can be expressed in terms of the intrinsic noise sources and the transconductance as explained in [66], increases with the gate overdrive due to the analogous trend of $S_{ID}$ and $S_{IG}$.

It can be observed that in spite of the outstanding differences observed in $S_{ID}$ and $S_{IG}$ with the SBH reduction, the net effect on $NF_{min}$ is counterbalanced by the increase of the device transconductance. At low currents (i.e., low $V_{GS} - V_T$), regardless of the SBH, the device exhibits excellent values of the intrinsic $NF_{min}$: from a quantitative point of view, less than 0.4 dB for barrier height equal to 0.15 eV and the corresponding $f_T$ of 80 GHz. $NF_{min}$ data of state-of-the-art conventional MOSFET with similar characteristics are included in Fig. 10 a for comparison [67–69]. To allow the comparison these data together with the Monte Carlo results are plotted as function of the drain current. The values obtained for $NF_{min}$ in the SB-MOSFET are in the range or only slightly higher than those corresponding to conventional MOSFETs. Only for a gate overdrive larger than 1 V $NF_{min}$ is slightly degraded when the barrier height is reduced, obtaining 0.9 dB for $V_{ov}$ = 1.456 V, which corresponds to the $f_T$ peak of 103 GHz for the lower SBH. $NF_{min}$ also shows the typical increase with frequency, as it can be seen in the inset of Fig. 8a, that depicts this FoM but for two additional values of frequency.

Fig. 10b shows the absolute value and the phase of the optimum generator reflection factor as function of the gate overdrive at 6 GHz. The knowledge of these two noise parameters is advantageous for achieving the noise matching of the device by using standard circuit simulators. The magnitude of $\Gamma_{opt}$ is practically independent on the SBH, being close to 1, for low $V_{ov}$ values. From the results obtained it can be inferred that, as $V_{ov}$ is increased, the magnitude of $\Gamma_{opt}$ slightly reduces and is improved with the SBH reduction, suggesting that a SB-MOSFET with lower barrier heights would allow an easier practical matching for optimal noise conditions. The phase of $\Gamma_{opt}$ presents a lineal dependency on frequency and increases with the gate overdrive, and is also strongly influenced by the SBH. The general trends observed with the gate bias for the absolute value and the phase of $\Gamma_{opt}$ are analogous to that showed experimentally [51] and by means of Monte Carlo simulation [26] for conventional SOI MOSFETs.

As our interest is to focus on the differential aspects in terms of microscopic noise sources and dynamic parameters and the impact of the SBH, we can analyze in depth this behaviour by relating $\Gamma_{opt}$ to the optimum admittance $Y_{opt} = G_{opt} + jB_{opt}$. The real and imaginary parts of this last quantity have been expressed in terms of the normalized $P$, $R$ and $C$ noise parameters [70]. Taking this into account, it is possible to express $G_{opt}$ and $B_{opt}$ in terms of the microscopic noise sources and the admittance parameters, which is more convenient in this context since such quantities are directly provided by the Monte Carlo simulation. In this way, after basic straightforward calculations we can obtain:

$$G_{opt} = |Y_{21}|\sqrt{\frac{S_{IG}}{S_{ID}} - \frac{\mathrm{Im}^2(S^*_{IGID})}{S^2_{ID}}} \quad (1)$$

$$B_{opt} = |Y_{21}|\frac{\mathrm{Im}(S^*_{IGID})}{S_{ID}} - |Y_{11}| \quad (2)$$

By the inspection of the different terms involved in these calculations, and their dependence on SBH, we can conclude that the previously stated reduction of $|\Gamma_{opt}|$ (as $V_{ov}$ is increased over 0.5 V and also when the SBH is reduced) can be associated mainly to the increment with of $G_{opt}$ (Fig. 11a). From Eq. (1) it can be deduced, taking into account our results, that this behaviour can be related to the enhancement of the transconductance (which is practically coincident with $|Y_{21}|$). On the other hand, the phase of $\Gamma_{opt}$ is basically influenced by the imaginary part of the optimum admittance, $B_{opt}$, and its behaviour (the increase as SBH is decreased) can be attributed for the most part to the second term of Eq. (2), this is, the larger values of $C_{gs}$ (related to $|Y_{11}|$), indicating that the larger control of the channel charge by the gate terminal accounts also for a increase in this quantity.

Fig. 11b exhibits the noise resistance, $R_n$, and the associated gain, $G_{ass}$ [64,70], as a function of the gate overdrive for the three different SBH values under consideration and for a constant applied drain bias equal to $V_{DS}$ = 2.0 V. $R_n$ measures the sensitivity of the noise figure when the source admittance differs from its optimum value, being an important parameter for optimizing the microwave noise performance of MOSFET's [51]. It can be seen that, when reducing $V_{ov}$ under 0.5 V, an increase in $R_n$ is observed, which can be attributed to the low value of the intrinsic transconductance, as in the case of conventional MOSFETs [51]. For gate overdrive values over 0.5 V, an almost constant noise resistance value (around $3 \times 10^{-3}\ \Omega\,\mathrm{m}$) is obtained, with just a slight dependence on the Schottky barrier height. Although in our case the four noise parameters have been obtained by means of the procedure explained in [64], the $R_n$ results are completely in accordance with the simplified assumption for the noise resistance in terms of $S_{ID}$ and $g^2_m$ [51,71]. In this case, both $S_{ID}$ and $g^2_m$ tend to neutralize each other: i.e., the improved dynamic performance for lower Schottky barrier height minimizes the effect of the increase of the intrinsic drain current noise power spectral density, thus not penalizing the noise resistance values. The associated gain, $G_{ass}$,

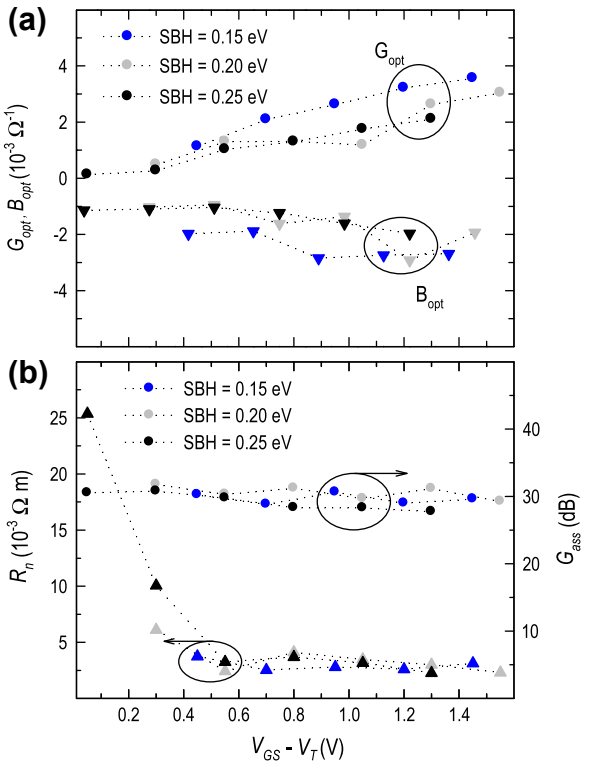


**Fig. 11.** Optimum noise conductance $G_{opt}$ (circles) and susceptance $B_{opt}$ (triangles), versus $V_{GS} - V_T$ for $V_{DS}$ = 2 V at 6 GHz (a) and the three different values of SBH. Noise resistance, $R_n$ (triangles) and associated gain, $G_{ass}$ (circles), versus $V_{GS} - V_T$ for $V_{DS}$ = 2 V at 6 GHz (b) for the three different barrier heights.

indicates the available gain of the transistor when it is matched for minimum noise figure conditions ($NF_{min}$). It can be noticed that for all the Schottky barrier height values considered $G_{ass}$ tends to slightly decrease with $V_{ov}$. Moreover there is not a significant influence of the barrier height on $G_{ass}$ (just a slight enhancement with the SBH decrease), indicating an analogous capability of the device of amplifying a signal under minimum noise conditions when the SBH is reduced. The values obtained for the simulated $G_{ass}$ are quite large, demonstrating the suitability of this technology for RF applications. As an example, the transistor with SBH equal to 0.15 eV presents (for $V_{ov}$ = 0.7 V, $V_{DS}$ = 2.0 V, corresponding to an $I_D$ = 184 μA μm$^{-1}$) a transconductance of 510 S m$^{-1}$ together with a very attractive RF noise values such as $NF_{min}$ of 0.44 dB and $G_{ass}$ = 30.2 dB at 6 GHz. As a result, although lowering the SBH strongly modifies the microscopic transport in the channel, which is translated into a deterioration of the intrinsic noise performance, it has only little impact on the circuital noise performance of the transistors for low-power applications due to the enhancement of the dynamic performance. This is an important result since a reduced SBH is imperative for the success of SB-MOSFET technology.

## 5. Conclusions

A Monte Carlo investigation of the influence of the SBH on the dynamic and noise performance of SB-MOSFETs has been presented. Our results show that the SBH reduction favours an outstanding enhancement of the transconductance and to a lesser extent of the cut-off frequency, as well as the reduction of non-quasistatic parameters such as the intrinsic channel resistance or the propagation delay time. We have found that the larger transconductance values for low SBH are based on the increase of electron concentration (for a given $V_{GS}$ voltage step) close to the source, together with a more effective control of the gate electrode over drain current that strongly reduces the transconductance delay time. A larger value of SBH affects significantly the movement of carriers within the channel. A SBH rise yields to a more pronounced two dimensional effects which in turn worsens the transit times and the mean free path of carriers crossing the channel.

The SBH reduction deteriorates the intrinsic noise sources due to the larger current levels, the appearance of extremely hot carriers inside the device and the reduced phonon scatterings. However, the main noise FoM, $NF_{min}$, achieves excellent values that are only slightly degraded with the reduction of the Schottky barrier height for large $V_{GS}$ conditions thanks to the above-mentioned improvement in the dynamic performance. The analysis of $\Gamma_{opt}$ suggests that an SB-MOSFET featuring a low barrier height would allow an easier practical matching for optimal noise conditions. Other relevant noise parameters such as $R_n$ and $G_{ass}$ do not seem to be significantly influenced by a SBH reduction. In general, reducing the effective barrier height means a noticeably improved static and dynamic performance, not penalizing the noise figures of merit of SB-MOSFETs. The results demonstrate that SB-MOSFET technology with low effective barrier heights may be an exceptional solution for the design of low-power low-noise high frequency applications.

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## References

[1] Lepselter MP, Sze SM. SB-IGFET: an insulated-gate field-effect transistor using Schottky barrier contacts for source and drain. Proc IEEE 1968;56:1400.
[2] Tucker JR, Wang C, Carney PS. Silicon field-effect transistor based on quantum tunnelling. Appl Phys Lett 1994;65:618–20.
[3] Kedzierski J, Xuan P, et al. A 20 nm gate-length ultra-thin body p-MOSFET with silicide source/drain. Superlatt Microstruct 2000;28:445–52.
[4] The international technology roadmap for semiconductors. San Jose, CA; 2009. <http://www.public.itrs.net>.
[5] Khater MH et al. High-κ/metal-gate fully depleted SOI CMOS with single-silicide Schottky source/drain with sub-30-nm gate length. IEEE Electron Dev Lett 2010;31:275–7.
[6] Jang M, Kim Y, et al. Formation of erbium-silicide as source and drain for decananometer-scale Schottky barrier metal-oxide-semiconductor field-effect transistors. Mater Sci Eng 2004;114:51–5.
[7] Connelly D, Faulkner C, Grupp DE. Performance advantage of Schottky source/drain in ultrathin body silicon on insulator and dual-gate CMOS. IEEE Trans Electron Dev 2003;50:1340–5.
[8] Larson JM, Snyder JP. Overview and status of metal S/D Schottky-barrier MOSFET technology. IEEE Trans Electron Dev 2006;53:1048–58.
[9] Choi S-J, Choi C-J, Kim J-Y, Jang M, Choi Y-K. Analysis of transconductance (gm) in Schottky-barrier MOSFETs. IEEE Trans Electron Dev 2011;58:427–32.
[10] Fritze M et al. High-speed Schottky-barrier pMOSFET with $f_T$ = 280 GHz. IEEE Electron Dev Lett 2004;25:220–2.
[11] Sugino M, Akers LA, Rebeschini ME. Latchup-free Schottky-barrier CMOS. IEEE Trans Electron Dev 1983;30:110–8.
[12] Swirhun SE, Sangiorgi E, Weeks AJ, Swanson RM, Saraswat KC, Dutton RW. A VLSI-suitable Schottky-barrier CMOS process. IEEE Trans Electron Dev 1985;32:194–202.
[13] Calvet LE, Luebben H, et al. Suppression of leakage current in Schottky barrier metal-oxide-semiconductor field-effect transistors. J Appl Phys 2002;91:757–9.
[14] Östling M, Luo J, Gudmundsson V, Hellström P-E, Malm BG. Nanoscaling of MOSFETs and the implementation of Schottky Barrier S/D contacts. In: Proc. 27th international conference on microelectronics, MIEL; 2010.
[15] Choi S-J, Han J-W, Kim S, Moon D-I, Jang M, Choi Y-K. Dopant-segregated Schottky source/drain FinFET with a NiSi FUSI gate and reduced leakage current. IEEE Trans Electron Dev 2010;57:2902–6.
[16] Vega RA, King LT-J. DSS MOSFET with tunable SDE regions by fluorine pre-silicidation ion implant. IEEE Electron Dev Lett 2010;31:785–7.

[17] Valentin R, Dubois E, et al. RF small-signal analysis of Schottky-barrier p-MOSFET. IEEE Trans Electron Dev 2008;55:1192–202.
[18] Huang C-K, Zhang WE, Yang CH. Two-dimensional numerical simulation of Schottky barrier MOSFET with channel length to 10 nm. IEEE Trans Electron Dev 1998;45:842–8.
[19] Guo J, Lundstrom MS. A computational study of thin-body, double-gate, Schottky barrier MOSFETs. IEEE Trans Electron Dev 2002;49:1897–902.
[20] Zeng L et al. A computational study of dopant-segregated Schottky barrier MOSFETs. IEEE Trans Nanotechnol 2010;9:108–13.
[21] Winstead B, Ravaioli U. Simulation of Schottky barrier MOSFET's with a coupled quantum injection/Monte Carlo technique. IEEE Trans Electron Dev 2000;47:1241–6.
[22] Valentin R et al. Optimization of RF performance of metallic source/drain SOI MOSFETs using dopant segregation at the Schottky interface. IEEE Electron Dev Lett 2009;30:1197–9.
[23] Xia Z, Du G, et al. Investigation of RF performance of nano-scale ultra-thin-body Schottky-barrier MOSFETs using Monte Carlo simulation. IEEE Conf Electron Dev Solid-State Circ 2005:305–8.
[24] Saha AR, Chattopadhyay S, Bose C, et al. Technology CAD of silicided Schottky barrier MOSFET for elevated source–drain engineering. Mater Sci Eng 2005;124:424–30.
[25] Jacoboni C, Lugli P. The Monte Carlo Method for semiconductor device simulation. Wien: Springer-Verlag; 1989.
[26] Rengel R et al. A microscopic interpretation of the RF noise performance of fabricated FDSOI MOSFETs. IEEE Trans Electron Dev 2006;53:523–32.
[27] Lusakowski J, Martín MJ, Rengel R, et al. Quasiballistic transport in nanometer Si metal-oxide-semiconductor field-effect transistors: experimental and Monte Carlo analysis. J Appl Phys 2007;101:114511.
[28] Sun L et al. Monte Carlo simulation of Schottky contact with direct tunnelling model. Semicond Sci Technol 2003;18:576–81.
[29] Matsuzawa K, Uchida K, Nishiyama A. A unified simulation of Schottky and ohmic contacts. IEEE Trans Electron Dev 2000;47:103–8.
[30] Rengel R, Pascual E, Martín MJ. Injected current and quantum transmission coefficient in low-Schottky barriers: WKB and airy approaches. IEEE Trans Electron Dev Lett 2007;18:171–3.
[31] Pascual E, Rengel R, Martín MJ. Microscopic modelling of reverse biased Schottky diodes: influence of non-equilibrium transport phenomena. Semicond Sci Technol 2007;22:1003–9.
[32] Pascual E et al. Enhanced carrier injection in Schottky contacts using dopant segregation: a Monte Carlo research. Semicond Sci Technol 2009;24:025022.
[33] Pascual E, Rengel R, Martín MJ. Current drive in n-type Schottky barrier MOSFETs: a Monte Carlo study. In: IEEE proceedings of the 2009 Spanish conference on electron devices; 2009.
[34] Rengel R et al. A Monte Carlo investigation of the RF performance of partially-depleted SOI MOSFETs. Semicond Sci Technol 2006;21:273–8.
[35] Knoch J et al. On the performance of single-gated ultrathin-body SOI Schottky-barrier MOSFETs. IEEE Trans Electron Dev 2006;53:1669–74.
[36] Kinoshita A. Physics and technology of dopant-segregated Schottky (DSS) MOSFETs. In: Proc. silicon nanoelectronics workshop, SNW; 2007. p. 9–10.
[37] Yang Y et al. Variability induced by line edge roughness in double-gate dopant-segregated Schottky MOSFETs. IEEE Trans Nanotechnol 2011;10:244–9.
[38] Knoch J, Zhang M, Zhao QT, Lenk St, Mantl S, Appenzeller J. Effective Schottky barrier lowering in silicon-on-insulator Schottky-barrier metal-oxide-semiconductor field-effect transistors using dopant segregation. Appl Phys Lett 2005;87:263505.
[39] Colinge J-P. Silicon-on-insulator technology. Materials to VLSI. 2nd ed. Norwell, MA; 1997.
[40] Gamiz et al. Electron transport in silicon-on-insulator devices. Solid State Electron 2001;45:613–20.
[41] Vega RA, Liu T-JK. A comparative study of dopant-segregated Schottky and raised source/drain double-gate MOSFETs. IEEE Trans Electron Dev 2008;55:2665–77.
[42] Reckinger N et al. Low Schottky barrier height for ErSi2-$x$/$n$-Si contacts formed with a Ti cap. J Appl Phys 2008;104:103523.
[43] Larrieu G et al. Arsenic-segregated rare-earth silicide junctions: reduction of Schottky barrier and integration in metallic n-MOSFETs on SOI. IEEE Trans Electron Dev Lett 2009;30:1266–8.
[44] Zhang Z et al. Schottky-barrier height tuning by means of ion implantation into preformed silicide films. IEEE Trans Electron Dev Lett 2007;28:565–7.
[45] Larrieu G, Dubois E. CMOS inverter based on Schottky source–drain MOS technology with low-temperature dopant segregation. IEEE Trans Electron Dev Lett 2011;32:728–30.
[46] Xiong SY, King TJ, Bokor J. A comparison study of symmetric ultrathin-body double-gate devices with metal source/drain and doped source/drain. IEEE Trans Electron Dev 2005;52:1859–67.
[47] Vega RA. On the modelling and design of Schottky field-effect transistors. IEEE Trans Electron Dev 2006;53:866–74.
[48] Zhu G et al. A compact model for undoped silicon-nanowire MOSFETs with Schottky-barrier source/drain. IEEE Trans Electron Dev 2009;56:1100–9.
[49] Schwarz M et al. Analytical 2D model for the channel electric field in undoped Schottky barrier double-gate MOSFET. MIXDES 2010.
[50] Berroth M, Bosch R. Broad-band determination of the FET small-signal equivalent-circuit. IEEE Trans Microwave Technol 1990;38:891–5.
[51] Dambrine G et al. High-frequency four noise parameters of silicon-on-insulator-based technology MOSFET for the design of low-noise RF integrated circuits. IEEE Trans Electron Dev 1999;46:1733–41.
[52] Manku T. Microwave CMOS – device physics and design. IEEE J Solid-State Circ 1999;34:277–85.
[53] Raskin JP et al. Accurate SOI MOSFET characterization at microwave frequencies for device performance optimization and analogue modelling. IEEE Trans Electron Dev 1998;45:1017–25.
[54] Lee S, Yu HK. Determining non-quasi-static small-signal equivalent circuit of a RF silicon MOSFET. Solid State Electron 2001;45:359–64.
[55] Rengel R, Pardo D, Martín MJ. A physically based investigation of the small-signal behaviour of bulk and fully-depleted silicon-on-insulator MOSFETs for microwave applications. Semicond Sci Technol 2004;19:634–43.
[56] Emam M, Vanhoenacker-Janvier D, Raskin JP. Effect of gate oxide scaling on RF performance of SOI MOSFET. In: IEEE proceedings of the 11th topical meeting on silicon monolithic integrated circuits in RF systems, SiRF; 2011. p. 73–6.
[57] Chen CL et al. Improvement of SOI MOSFET RF performance by implant optimization. IEEE Microwave Wire Compon Lett 2010;20:271–3.
[58] Wong H, Man KF, Poon MC. Modelling of saturation transconductance for short-channel MOSFETs. Solid-State Electron 1996;39:1401–4.
[59] Rengel R, Martín MJ. Electronic transport in laterally asymmetric channel MOSFET for RF analog applications. IEEE Trans Electron Dev 2010;57:2448–54.
[60] Urban C et al. Radio-frequency study of dopant-segregated n-type SB-MOSFETs on thin-body SOI. IEEE Electron Dev Lett 2010;31:537–9.
[61] Urban C et al. Small-signal analysis of high-performance p- and n-type SOI SB-MOSFETs with dopant segregation. Solid-State Electron 2010;54:877–82.
[62] Rengel R, Pardo D, Martin MJ. Towards the nanoscale: influence of scaling on the electronic transport and small-signal behaviour of MOSFETs. Nanotechnology 2004;15:276–82.
[63] van der Ziel A. Noise in solid state devices and circuits. New York: Wiley; 1986.
[64] Pailloncy G et al. Noise modeling in fully depleted SOI MOSFETs. Solid-State Electron 2004;48:813–25.
[65] Clement N, Larrieu G, Dubois E. Low-frequency noise in Schottky-barrier-based nanoscale field-effect transistors. IEEE Trans Electron Dev 2012;59:180–7.
[66] Rengel R, Martín MJ, Danneville F. Microscopic modelling of RF noise in laterally asymmetric channel MOSFETs. IEEE Electron Dev Lett 2011;32:72–4.
[67] Dambrine G et al. Gallium arsenide and other semiconductor application symposium. EGAAS 2005;97:97–100.
[68] Pailloncy G et al. Impact of downscaling on high-frequency noise performance of bulk and SOI MOSFETs. IEEE Trans Electron Dev 2004;51:1605–12.
[69] Kuhn K, et al. A comparison of state-of-the-art NMOS and SiGe HBT devices for analog/mixed-signal/RF circuit applications. In: 2004 Symposium on VLSI technology; 2004. p. 224–5.
[70] Emam M et al. Experimental investigation of RF noise performance improvement in graded-channel MOSFETs. IEEE Trans Electron Dev 2009;56:1516–22.
[71] Asgaran S, Deen MJ, Chen C-H. Analytical modeling of MOSFETs channel noise and noise parameters. IEEE Trans Electron Dev 2004;51:2109–14.