INSTITUTE OF PHYSICS PUBLISHING SEMICONDUCTOR SCIENCE AND TECHNOLOGY
Semicond. Sci. Technol. **16** (2001) 939–946 PII: S0268-1242(01)26070-2

Monte Carlo analysis of dynamic and noise performance of submicron MOSFETs at RF and microwave frequencies

R Rengel, J Mateos, D Pardo, T González and M J Martín

Departamento de Física Aplicada, Universidad de Salamanca, Plaza de la Merced s/n. 37008 Salamanca, Spain

E-mail: raulr@gugu.usal.es

Received 8 June 2001
Published 10 October 2001
Online at stacks.iop.org/SST/16/939

Abstract

In this paper, an ensemble 2D bipolar Monte Carlo simulator is employed for the study of static characteristics, high-frequency response and noise behaviour in a 0.3 μm gate-length n-MOSFET in common source configuration. Short-channel effects, such as velocity overshoot in the pinch-off region, together with the appearance of hot electrons at the drain end of the channel are observed in the static characteristics. Admittance parameters and the small-signal equivalent circuit have been calculated in order to characterize the dynamic response of the device. The use of a bipolar simulator allows one to study the dynamics of both types of carriers simultaneously. While the static results are dominated by the electron transport, the contribution of holes mainly affects the drain–substrate capacitive coupling. The noise behaviour of the simulated MOSFET is also studied (up to 40 GHz) by means of different parameters, such as the spectral densities of the current fluctuations at the drain and gate terminals (and their cross-correlation), normalized α, β and C parameters and $NF_{\min}$. In the saturation regime, due to the presence of hot carriers, an increase in drain and gate noise with respect to the long-channel prediction has been found. Moreover, a stronger correlation between drain and gate noise is observed, especially at low drain current. Induced gate noise is found to play a crucial role in the determination of $NF_{\min}$ at high drain currents.

1. Introduction

In the last decade, CMOS devices have become an interesting alternative for consideration in the design of radio-frequency (RF) integrated circuits. It must be remarked that the high-frequency performance of Si MOSFETs (in terms of unity current gain frequencies, f_T, minimum noise figure, $NF_{\min}$, etc) will never reach that of advanced III–V FETs due to the poorer electron transport properties. However, the progressive downscaling of silicon MOS transistors has permitted one to obtain f_T of tens of GHz [1,2], and several RF CMOS circuits have already been demonstrated [3]. Unfortunately, the reduction in the gate length (L_g) to deep submicron dimensions involves the appearance of undesired short-channel effects [4]. Although some other silicon-based technologies, such as silicon-on-insulator (SOI) seem a very promising alternative, CMOS technology still presents the clear advantage of very low cost and high levels of integration, and its feasibility in the design of RF system-on-chip applications is beyond all doubt.

To succeed in designing RF and microwave CMOS low-noise applications, a detailed characterization of the high-frequency noise performance of sub-micron MOSFETs is required. Especially in the saturation region (which is the usual region of operation of MOSFETs for analog applications), it is necessary to determine accurately the drain and gate noise equivalent sources and their cross-correlation [3]. Precise

device models are of capital importance for the optimization of the device design. Unfortunately, the conventional long-channel noise models for MOSFETs underestimate the drain noise for short-channel devices, as evidenced by experimental data found in the literature [5, 6]. Therefore, it is crucial to use a model that reproduces exactly the carrier transport conditions inside the device. Due to this fact, the ensemble Monte Carlo (EMC) method [7] is the ideal tool to carry out the mentioned study. It intrinsically incorporates all the transport phenomena of interest (such as non-stationary effects or the appearance of hot carriers) in such devices, together with the possibility of simulating both types of carriers. The EMC method also allows the extraction of many interesting physical quantities, such as carrier concentration, energy, velocity, etc, and therefore to study the primary origin of electronic noise. This method has been successfully employed in the study of noise in many different devices [8–10].

The aim of this paper is to present an EMC study of noise in a sub-micrometer gate-length MOSFET device under saturation conditions, focusing our analysis in the RF and microwave range, that is, up to 40 GHz [11]. The paper is organized as follows. In section 2, the simulated structure and the features of our Monte Carlo simulator are presented. In sections 3.1 and 3.2, the static characteristics and dynamic response of the device are studied. The noise sources are investigated in section 3.3 by means of the calculation of the spectral densities of current fluctuations in the gate and drain contacts, α, β and C parameters and minimum noise figure. To the authors' knowledge, this work represents the first attempt to calculate these noise parameters for a bulk MOSFET by using an ensemble bipolar Monte Carlo simulator. Finally, the main conclusions of this paper are presented.

2. Simulated device and Monte Carlo model

The geometry and doping levels of the simulated n-channel silicon MOSFET are shown in figure 1. The gate length is 0.3 μm, and the doping concentration of the p-substrate equals 2×10^{16} cm^{-3}. The source and drain n^+ regions are 0.3 μm long, with a doping concentration of 5×10^{17} cm^{-3}. Both parameters, together with the lateral position of the contacts, have been chosen in order to minimize the CPU time while ensuring carrier thermalization before reaching the drain contact. Even if these values may not correspond exactly to those employed in fabricated devices, their modification just leads to a change in the resistance of the ohmic regions next to the contacts; an effect that can be compensated for in a post-processing stage by means of considering a series resistance in the contacts [12]. Furthermore, since electron transport in a MOSFET depends basically on the inversion layer under the oxide, the relatively 'low' doping of the source and drain regions does not change the results significantly. A p^+ region with a doping concentration of 2×10^{17} cm^{-3} has been considered at the bottom of the device to perform the substrate contact. The built-in potential considered for the MOS structure is 0.95 eV. The oxide thickness is 10 nm, which is within the technological limits usually employed in MOSFETs for the considered L_g [4]. Due to the dimensions and the L_g considered in this structure, short-channel effects (such as excess drain noise) are expected to be observed. The source

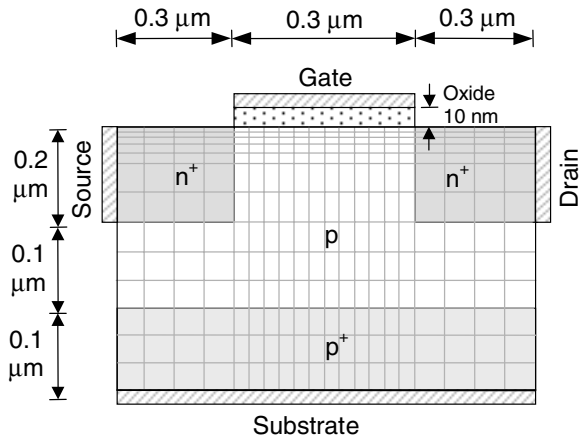

Figure 1. Scheme of the simulated device. The grid does not correspond to the real dimensions; it is just indicative of the areas where the dimensions of the meshes are smaller.

and substrate terminals are short-circuited, and the device is considered to operate in common-source configuration, as in the majority of high-frequency applications [13].

The calculations are performed by means of a 2D semiclassical EMC simulator, consistently coupled with a two-dimensional Poisson solver. Many authors consider holes in a quasi-static approximation when solving the Poisson equation [14], which is physically plausible for the static analysis of MOSFETs. However, when dealing with dynamic and noise behaviour, the consideration of the simultaneous self-consistent dynamics of both types of carriers becomes necessary. Thus, in our case both electrons and holes are simulated as particles [15]. Due to this fact, it is possible to evaluate the influence of substrate holes on the dynamic response and noise behaviour of the device. The band structure of silicon is considered to be formed by nonparabolic, anisotropic X and L valleys in the conduction band, and heavy- and light-hole subbands in the valence band. The scattering mechanisms and parameters for electrons and holes may be found in [16]. The temperature considered in the simulation is 300 K. The device is divided into meshes 50–100 Å long and 10–100 Å wide in order to solve accurately the Poisson equation in the whole device including the gate oxide. Due to the high concentration of the inversion layer, the size of the meshes is smaller in the region under the oxide (figure 1). The time step used to solve the Poisson equation is 2.5 fs, and the number of simulated particles varies from 10 500 to 12 000 electrons and 6500 to 7500 holes depending on the bias point. In order to realise an accurate noise calculation, a simulation time of 500 ps for each bias point has been necessary. Dirichlet conditions (fixed potential) are considered at the four terminals. At the oxide–semiconductor interface the continuity of the displacement vector normal to the surface is taken into account. The source, drain and substrate contacts are considered to be ohmic [17].

In order to perform a correct calculation of the admittance (Y) parameters and the spectral densities of current fluctuations, an accurate calculation of the electrode currents is necessary. The Ramo–Shockley theorem [18] is employed for this purpose. With this technique, the contribution of every particle inside the simulated device to the total current (formed

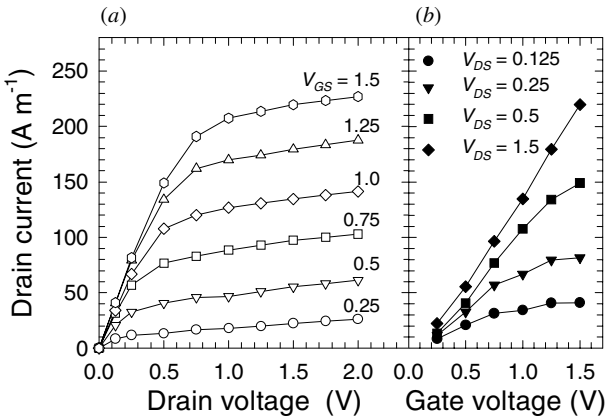

Figure 2. (*a*) Output and (*b*) transfer characteristics of the simulated MOSFET.

by the electron and hole conduction terms and the displacement term) [9] is taken into account, and the calculated values for the instantaneous currents at the terminals are much more accurate [19].

3. Results

3.1. Static characteristics

Figure 2(*a*) shows the drain current (I_D) versus drain voltage (V_{DS}) characteristics for different gate voltages (V_{GS}). In figure 2(*b*), the transfer characteristics (I_D versus V_{GS}) are also plotted. The dependence of I_D with V_{DS} is associated with the evolution of the inversion layer with the drain voltage. In figure 3, the electron concentration in the channel region 15 nm under the oxide is shown in a contour graph for three different V_{DS} (0.25, 0.5 and 1.0 V) and a value of 0.5 V for V_{GS}. For low drain voltages, the inversion layer extends over the entire channel (figure 3(*a*)). The behaviour of the device is purely resistive, and the I_D–V_{DS} characteristic exhibits a linear dependence. When the drain voltage increases, the inversion layer induced by the gate begins to progressively reduce its concentration at the drain side of the channel (figure 3(*b*)) due to the increasing length of the depletion region associated with the drain–substrate junction. Finally, for $V_{DS} = 1$ V, the inversion layer disappears at the drain side and the pinch-off phenomenon can be clearly observed (figure 3(*c*)). For higher V_{DS}, the depletion region near the drain increases its width and is responsible for the voltage drop exceeding the saturation voltage. It has to be remarked that for the MOSFET under study, the length of the pinch-off region is not negligible as compared to the total gate length, as can be observed in figure 3(*c*). This provokes that the drain current in the saturation region is not constant with the drain voltage, and, as a consequence, a slight increment in the current level in the saturation regime is observed. This effect typically appears in devices with a submicrometric gate length [4]. Since we are interested in studying the device behaviour in the saturation regime, in most of the results shown in this paper we have considered a value of V_{DS} equal to 1.5 V, and we have varied V_{GS} in order to obtain the dependence of the different parameters with the drain current.

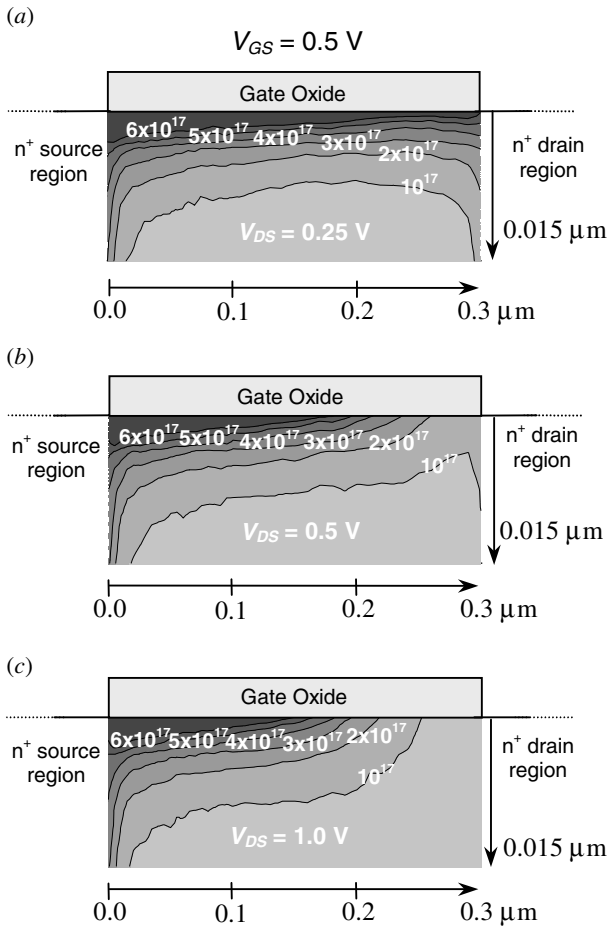

Figure 3. Electron concentration (in cm^{-3}) in the channel under the oxide for $V_{GS} = 0.5$ V and different drain voltages: (*a*) 0.25 V, (*b*) 0.5 V and (*c*) 1.0 V.

The average velocity along the channel and the energy of electrons in the inversion layer are shown in figure 4 for a fixed V_{DS} of 1.5 V and two different bias values in the gate, $V_{GS} = 0.25$ V (figure 4(*a*)) and $V_{GS} = 1.5$ V (figure 4(*b*)). Velocity overshoot is observed in the pinch-off region, as expected for a short-channel MOSFET [14] (v_{sat} corresponds to the saturation value of electron velocity in bulk Si). Accordingly, hot electrons appear at the drain end of the channel, reaching energies even larger than 0.5 eV. Both effects are due to the fact that the carrier transport takes place under a very high lateral electric field. The value of this electric field at the drain side of the gate increases when V_{GS} is reduced, leading to the widening of the overshoot region and the increase of the maximum value of the energy for low V_{GS}, as it can be observed in figure 4. Moreover, it can also be checked that the length and doping concentration of the drain n^+ region are wide and high enough respectively, to allow the thermalization of electrons before reaching the contact.

3.2. Dynamic response

The ac behaviour of a MOSFET device can be represented by the complex frequency-dependent two-port Y parameters [20]. In this work the Y parameters are obtained directly from our Monte Carlo simulation by means of the following

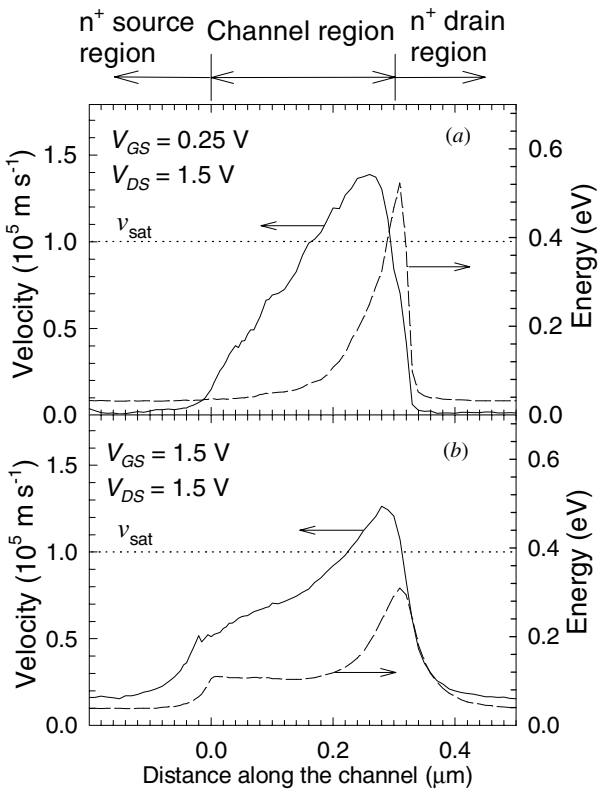

Figure 4. Average velocity (solid curve) and energy (dashed curve) of electrons in the inversion layer for $V_{DS} = 1.5$ V and two different gate voltages, (*a*) $V_{GS} = 0.25$ V and (*b*) $V_{GS} = 1.5$ V.

procedure [21]. First of all, a stationary bias point is chosen. Secondly, small step voltage perturbations are applied separately at the gate and drain terminals (ΔV_{GS} and ΔV_{DS} respectively), and the simulation takes place until stationary conditions are reached again. By Fourier transformation of the transient response (bearing in mind that the EMC method allows one to record the instantaneous values of the terminal currents for each time step) the four Y parameters are obtained. The values of the applied voltage steps must be large enough to dominate over numerical and physical noise but small enough to avoid harmonic generation. For instance, for the bias points corresponding to $V_{GS} = 1.0$ V and $V_{DS} = 1.5$ V, ΔV_{GS} and ΔV_{DS} have been chosen to be equal to 0.1 and 0.25 V, respectively.

Figure 5 shows the real and imaginary parts of the Y parameters for the bias point corresponding to V_{GS} 0.5 V and V_{DS} 1.5 V (in the saturation region) as a function of frequency up to 40 GHz. The sign and frequency dependence of the Y parameters are in good agreement with measured data found in the literature for other submicron MOSFETs [13, 22]. Nevertheless, the Y parameters give little information about the physics of the device. The small-signal equivalent circuit (SSEC) is frequently employed in order to have a more physical representation of the device. We considered the typical intrinsic SSEC for a FET transistor in common source configuration, whose different elements were calculated from the Y parameters [23]. It must be pointed out that the results obtained from our MC simulator for the SSEC parameters are frequency independent up to more than 40 GHz, which

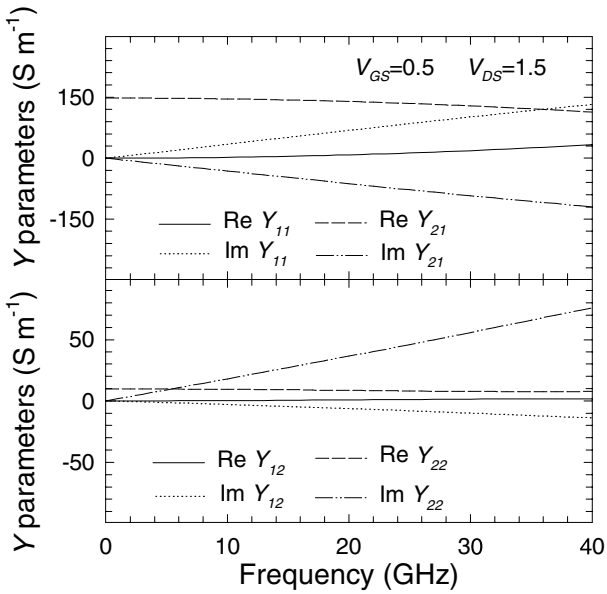

Figure 5. Admittance parameters as a function of frequency for $V_{GS} = 0.5$ V and $V_{DS} = 1.5$ V.

confirms the validity of the proposed equivalent circuit in the considered frequency range.

Figure 6(*a*) shows the values obtained for the SSEC capacitances as a function of drain current for a value of V_{DS} of 1.5 V, in the saturation region. As it can be observed, the gate-to-source capacitance (C_{GS}) takes the highest values. The gate-to-drain capacitance (C_{GD}) takes the smallest values, but its influence increases as the current level does. This behaviour can be easily explained by means of the analysis of the static characteristics and the corresponding carrier concentration in the inversion layer of the device (figure 3). In the pinch-off regime, the source end of the channel accounts for the bigger part of the inversion charge (figure 3(*c*)), and C_{GS} is the dominant capacitance (especially for I_D lower than 150 A m^{-1}). Nevertheless, for constant V_{DS}, as the gate voltage increases the pinch-off region becomes shorter, and the inversion charge tends to be more balanced between the drain and source, and, as a consequence, the difference between C_{GS} and C_{GD} is reduced [4]. It must be remarked that when lowering the gate voltage ($I_D < 40$ A m^{-1}) C_{GS} strongly decreases, since for low gate voltages the device operates in the moderate inversion region. In this case, the EMC method allows us to check that the charge in the channel is not so sensitive to variations of the applied voltage as for higher V_{GS}, as predicted by theory [4]. Concerning the drain-to-source capacitance (C_{DS}), it slightly varies with the gate voltage, as it can be observed in figure 6(*a*). In order to study the influence of substrate holes on the SSEC capacitances, we performed an alternative calculation of the capacitances neglecting the contribution of the hole current to the total current during the transient response. Very small differences where found for C_{GS} and C_{GD}, since they strongly depend on the inversion layer charge. Nevertheless, when the contribution of holes to the total current is precluded, a significant reduction in the value of C_{DS} takes place, as can be seen in figure 6(*a*). Therefore, holes are found to play a significant role in the dynamic behaviour mainly related to the drain–substrate capacitive coupling.

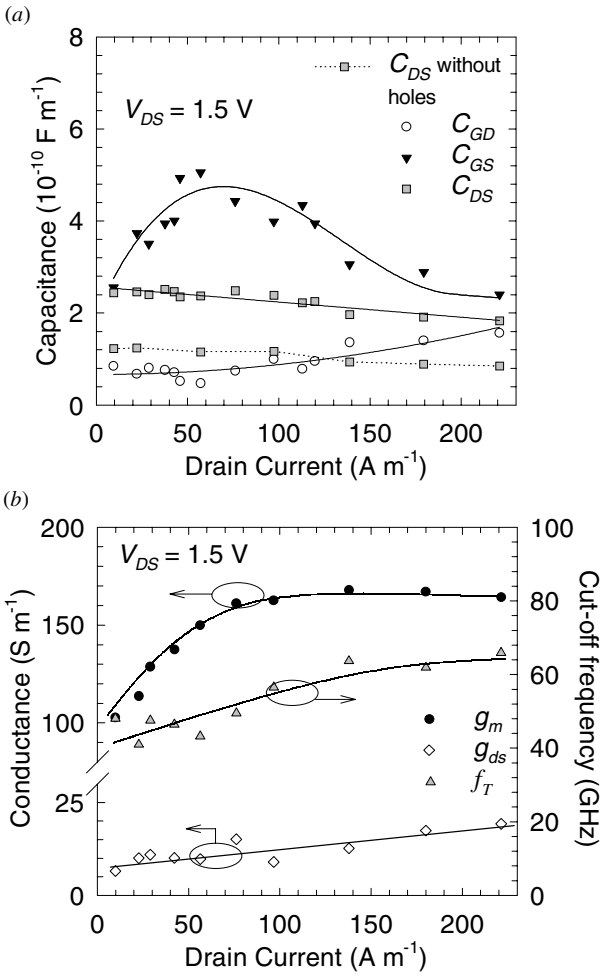

Figure 6. (*a*) SSEC capacitances versus I_D for $V_{DS} = 1.5$ V. Curves show the tendency of the different parameters. The dotted squares curve shows the results obtained for C_{DS} when the contribution of holes to the total current is neglected. (*b*) g_m, g_{ds} and f_T as a function of I_D for $V_{DS} = 1.5$ V. Tendency curves are also plotted.

Figure 6(*b*) shows the calculated values of the transconductance (g_m), output conductance (g_{ds}) and intrinsic cut-off frequency (f_T) as a function of drain current for V_{DS} 1.5 V. The cut-off frequency is given by [4]:

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{1}$$

g_m represents the variation of I_D with the applied V_{GS} for a given V_{DS}; as the current level increases, its value increases until it reaches a maximum value (around 160 S m^{-1} for I_D equal to 140 A m^{-1}), corresponding to the strong inversion region in saturation [4]. With regard to the influence of SSEC capacitances on f_T in the saturation regime, due to the higher value of C_{GS} this is the one that mainly limits f_T. As can be observed, f_T approximately follows the behaviour of g_m, taking into account that for low currents the lower values of g_m are partially compensated by the reduction of C_{GS} in the moderate inversion region. The maximum value of f_T is found to be equal to 65 GHz for I_D around 220 A m^{-1}. Concerning g_{ds}, it increases with the bias current, since for high I_D the device operates closer to the triode region (figure 2(*a*)). It has to be stressed that the EMC results obtained correctly reproduce the experimental behaviour of these parameters with the gate voltage [6].

3.3. Noise

A noisy two-port device in common source configuration may be represented by means of the intrinsic noiseless device together with two correlated noise current generators, one at the input (gate) and the other at the output (drain) of the device [20]. The noiseless device is represented by the Y parameters, which have been previously shown in section 3.2. The EMC method allows one to calculate the equivalent noise sources together with their correlation through the analysis of the current fluctuations at the gate and drain terminals, without making any assumption about their physical origin. Moreover, this method provides a microscopic understanding of these noise sources by means of the study of the internal mechanisms that control the carrier transport inside the device. This possibility represents a clear advantage as compared to other methods.

3.3.1. Spectral densities of current fluctuations. Figure 7 shows the spectral densities of the gate (S_{IG}) and drain (S_{ID}) current fluctuations and their cross-correlation (S_{IGID}) obtained from the EMC simulation as a function of frequency for $V_{DS} = 1.5$ V and two different gate voltages in the saturation region. It can be observed that the spectral density of the fluctuations of the drain current (S_{ID}) is almost independent of frequency, as corresponds to a thermal noise source. As was previously commented in section 3.1, the basic operation of a field-effect transistor consists in the modulation of a conducting channel by the gate terminal. Therefore, the device operates as a modulated resistor, and, as a consequence, thermal noise is expected to appear in the channel. Thus, S_{ID} has its origin in the thermal noise generated by the carriers in the channel region. The gate noise source, S_{IG}, can be associated with the capacitive coupling (to the gate) of charge fluctuations in the channel. In the high-frequency range, the MOSFET may be considered as an RC distributed network; the capacitive coupling to the gate represents the distributed capacitance, and the channel represents the distributed resistance [20].

Since both noise sources (S_{ID} and S_{IG}) have the same origin—the thermal noise in the channel—they must be correlated (S_{IGID}). S_{IG} exhibits an f^2 dependence, whereas the imaginary part of S_{IGID} increases proportionally to f (the real part of S_{IGID} is negligible at the frequencies shown). These dependencies obtained are in good agreement with those predicted by the theory for a MOSFET in general [20], and with the results given in the literature for other FET devices, like MESFETs [8] or HEMTs [24].

Concerning the drain noise, experimental data show that in a short-channel MOSFET an excessive drain noise appears as compared to the long-channel devices [5,6]. The long-channel theory predicts a value for S_{ID} in the saturation regime of [20]:

$$S_{ID} = 4k_B T \tfrac{2}{3} g_m. \tag{2}$$

Figure 8 shows the results obtained with our MC simulator together with the values of S_{ID} estimated by the long-channel

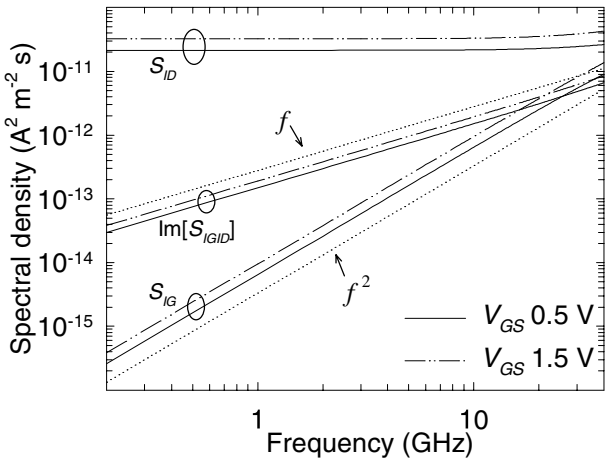

Figure 7. Spectral densities of current fluctuations and their cross-correlation as a function of frequency. f and f^2 dependencies are also plotted.

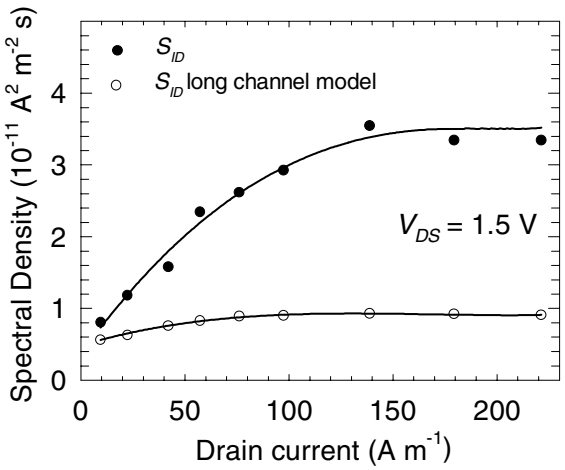

Figure 8. MC results and values predicted by the long-channel model for the spectral density of drain current fluctuations as a function of I_D for $V_{DS} = 1.5$ V. Tendency curves are also plotted.

theory (equation (2)) as a function of drain current for $V_{DS} = 1.5$ V, in the saturation region. It can be observed that our EMC results successfully provide an 'enhanced' drain noise, which increases with drain current. For low values of drain currents, S_{ID} increases rapidly, and the difference between the long-channel model and the EMC results becomes more outstanding as I_D increases. However, for I_D larger than 100 A m^{-1}, S_{ID} tends to saturate. The reason for this behaviour of S_{ID} can be associated with the presence of hot carriers. As we previously commented in section 3.1, hot carriers appear at the drain end of the channel due to the presence of a high electric field. In general, these hot carriers generate an excess noise with respect to the thermal equilibrium level, thus contributing to an increase of S_{ID} as compared to the long-channel prediction. When V_{GS} is raised, two opposing effects appear, on the one hand, the average energy of the carriers at the drain end of the channel reduces (figure 4); on the other, the amount of hot electrons increases due to the higher concentration of the inversion layer. The second effect is stronger at low I_D, thus leading to an important increase of S_{ID}, whereas for high current S_{ID} saturates, since both effects tend to compensate each other.

3.3.2. α, β, C parameters and $NF_{\min}$. To complete the analysis of the noise behaviour of the device, in addition to studying the spectral densities of the current fluctuations, it is of primary importance to use normalized noise parameters that allow direct comparison of the noise behaviour of different devices. The minimum noise figure, $NF_{\min}$, is the parameter most commonly employed for this purpose. Nevertheless, as a first step, normalized α, β and C parameters [20] have been determined. These parameters are equivalent to the generalized P, R and C for a FET in general, and they can give valuable information about the physical origin of noise [25]. α is a measure of the drain noise, β is associated with induced gate noise and C to the cross-correlation between drain and gate noise equivalent sources. These parameters can be calculated through the following expressions [25, 26]:

$$\alpha = \frac{S_{ID}}{4k_{\mathrm{B}}T|Y_{21}|} \tag{3}$$

$$\beta = \frac{S_{IG}|Y_{21}|}{4k_{\mathrm{B}}T|Y_{11}|^2} \tag{4}$$

$$C = \frac{\mathrm{Im}\,[S_{IGID}]}{\sqrt{S_{IG}S_{ID}}}. \tag{5}$$

Figure 9 shows the values of α, β and C as a function of drain current for a drain voltage of 1.5 V. Our EMC results for these parameters are almost independent of frequency in the frequency range considered. By comparing equations (2) and (3), since the transconductance corresponds practically to the magnitude of Y_{21} in saturation, it can be concluded that the value of α for the ideal long-channel device should be near 2/3. In our short-channel MOSFET higher values are obtained due to the excessive drain noise. Furthermore, it can be observed that α increases with the current level (S_{ID} increases more rapidly with V_{GS} than g_m). β is associated with the induced gate noise S_{IG} (equation (4)), and increases with the current level, as can be seen in figure 9(*b*). Furthermore, it significantly deviates from the long-channel prediction ($\beta \approx 0.3$). The induced gate noise has its primary origin in the charge fluctuations in the channel due to the thermal noise of carriers, and therefore it is increased by the presence of hot electrons. Moreover, as V_{GS} is raised, the higher amount of hot carriers leads to the augmentation of the fluctuations of charge in the channel, and, as a consequence, β increases. Therefore, the presence of hot electrons leads to an increase not only of α, but of β too, as suggested by van der Ziel [20] and confirmed by our simulation results. C is the correlation factor; the real part of S_{IGID} has been found to be roughly zero in the frequency range under study. It is important to remark that this result confirms that the drain–gate correlation coefficient is completely imaginary, as it is usually considered in theoretical models for FETs in general. Its theoretical value for a long-channel device is 0.395 [20]. In our case, our EMC simulator provides values up to 0.7, which also indicates that the ideal relationships fail to predict the actual values of the correlation factor, since a stronger correlation between gate and drain noise sources exists in a short-channel MOSFET

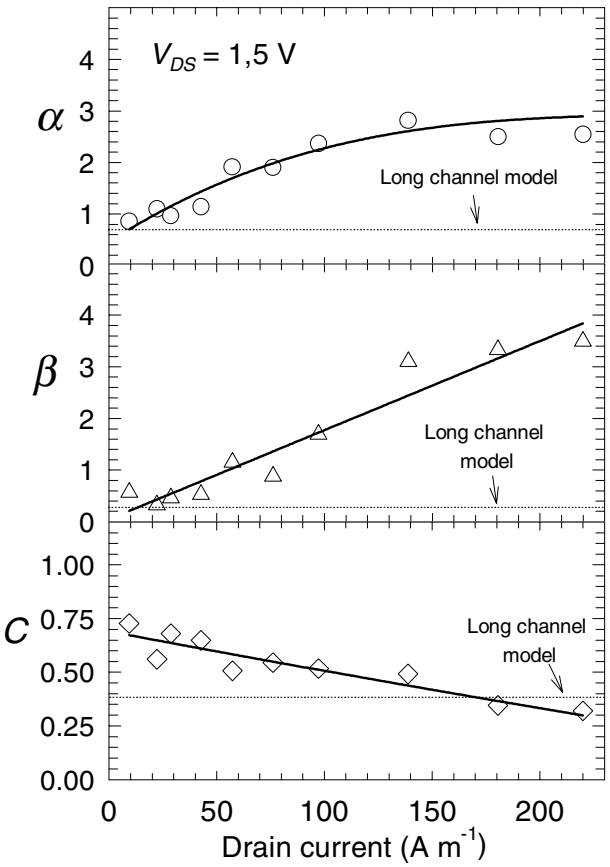

Figure 9. α, β, and C parameters as a function of drain current for $V_{DS} = 1.5$ V. Tendency curves for the different parameters are also plotted. Long-channel predictions are also indicated.

mainly at low gate voltages. This result (in good agreement with the simulation results obtained by other authors by means of a hydrodynamic approach [27]) is due to the fact that in the pinch-off region electron transport is quasi-ballistic, and scattering mechanisms are not able to break the correlation between S_{IG} and S_{ID}. Nevertheless, for high I_D (especially over 100 A m^{-1}) the value of C decreases and it is closer to the long-channel prediction, which agrees with the lower average energy of electrons and the reduced width of the velocity overshoot region at high gate voltages (figure 4) indicating a more diffusive electron transport character.

Although α, β and C parameters provide useful information, as mentioned above, the most typical parameter for an experimental characterization of the global noise performance of a device is the minimum noise figure, $NF_{\min}$. This figure of merit indicates how the device increases the noise level of the signal that is being amplified. The intrinsic $NF_{\min}$ can be calculated using the following equations [28–30]:

$$NF_{\min} = 1 + 2R_n\left[G_{\rm cor} + G_{\rm opt}\right] \tag{6}$$

with

$$R_n(f) = \frac{S_{ID}}{4k_{\rm B}T|Y_{21}|^2} \tag{7}$$

$$G_{\rm cor} = {\rm Re}\left[Y_{11} - Y_{21}\frac{S^*_{IGID}}{S_{ID}}\right] \tag{8}$$

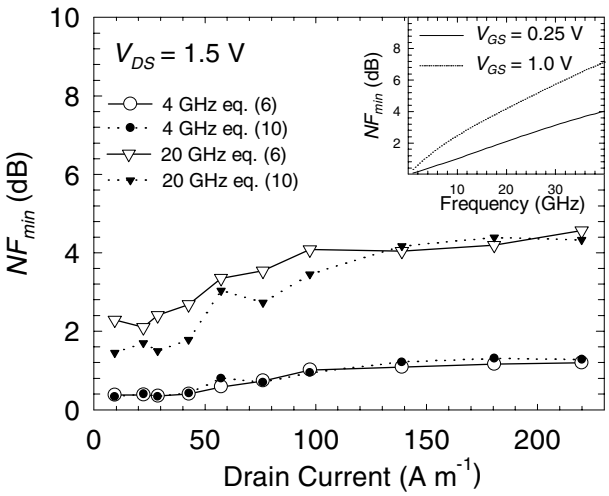

Figure 10. Minimum noise figure versus I_D for $V_{DS} = 1.5$ V at two different operating frequencies, 4 and 20 GHz. Inset shows the frequency dependence of $NF_{\min}$ for two different gate voltages.

and

$$G_{\rm opt} = \sqrt{|Y_{21}|^2\frac{S_{IG}}{S_{ID}} + |Y_{11}|^2 - 2{\rm Re}\left[Y_{11}Y^*_{21}\frac{S_{IGID}}{S_{ID}}\right] - \left({\rm Im}\left[Y_{11} - Y_{21}\frac{S^*_{IGID}}{S_{ID}}\right]\right)^2}. \tag{9}$$

Although equations (6)–(9) are an exact calculation for $NF_{\min}$, the minimum noise figure can be also calculated from α, β, and C parameters by means of the following approximation [31]:

$$NF_{\min} = 1 + 2\frac{f}{f_T}\sqrt{\alpha\beta(1 - C^2)}. \tag{10}$$

Figure 10 shows the intrinsic minimum noise figure as a function of drain current for 4 and 20 GHz and a drain voltage of 1.5 V, calculated exactly by means of equation (6) (white symbols) and through the approximation of equation (10) (black symbols). The dependence of $NF_{\min}$ on frequency (calculated through equation [6]) for two different values of V_{GS} and $V_{DS} = 1.5$ V is shown in the inset. In general, for both calculations it can be observed that, as expected, $NF_{\min}$ increases with the operating frequency. Furthermore, $NF_{\min}$ also increases with current, a fact that has been confirmed by experimental data [32].

Although equation (10) tends to underestimate the value of $NF_{\min}$ for low currents and high frequencies as compared to the results given by equation (6), in general equation (10) can be considered a good approximation to the exact calculation, allowing us to relate $NF_{\min}$ to α, β and C parameters. From our MC simulation results and bearing in mind equation (10), it can be concluded that the increase in $NF_{\min}$ with current can be attributed to the increase of α and β and the reduction in Cas the gate voltage increases. Furthermore, taking into account the values obtained for the β parameter, comparable or even higher than those obtained for α at high V_{GS} (figure 9), it becomes clear that induced gate noise plays a very important role in the determination of the minimum noise figure in the saturation regime, as confirmed by other authors [3]. It is also important to show that the improved C due to the ballistic transport of electrons through the channel (mainly at low V_{GS}) reduces the noise level of the devices.

4. Conclusions

An ensemble bipolar 2D Monte Carlo simulation of a n-MOSFET with a submicrometric gate length has been performed. The static response, dynamic behaviour and high-frequency noise of the device were studied. Velocity overshoot of electrons has been observed in the channel region near the drain, together with the appearance of hot carriers, which become crucial in the noise performance of the device. Moreover, for a constant V_{DS}, the width of the velocity overshoot region and the maximum of the average energy of electrons have been checked to decrease as V_{GS} increases.

The results obtained for the SSEC parameters reproduce correctly the experimental and theoretical behaviour of these parameters with the bias current. Nevertheless, it has been shown that neglecting the contribution of holes to the total current at the terminals leads to an important underestimation of C_{DS} for this structure.

Noise parameters (α, β, C and $NF_{\min}$) have been calculated (for the first time in a MOSFET by means of an EMC simulator) through the previously determined admittance parameters and noise spectral densities. The noise spectral densities, calculated by Fourier analysis of current fluctuations, show an increase in S_{ID} and a stronger correlation between source and drain fluctuations, S_{IGID}, with respect to the long-channel theory. This is related to excess noise generated by the presence of hot carriers in the saturation region. Nevertheless, the value of S_{ID} tends to saturate and the correlation reduces for high drain currents, due to the lower average energy of electrons at the drain end of the channel for high V_{GS}. As a consequence of the excessive drain noise observed, α, β and C show higher values than those predicted by the long-channel model, especially in the case of C at low currents, where the pinch-off region accounts for a big part of the channel. With regard to $NF_{\min}$, from the results obtained it can be asserted that the increase of $NF_{\min}$ with current is due to the increase of drain noise and induced gate noise and the reduction in the drain–gate correlation as the gate voltage increases. Furthermore, it has been shown that induced gate noise means a significant contribution to the minimum noise figure especially at high I_D in saturation.

In general, the results obtained demonstrate the capability of our EMC simulator to analyse the dynamic and noise performance of short-channel MOSFETs. However, in order to compare the simulation results with experimental measurements in fabricated devices, several real effects must be considered, like impact ionisation, interface states generation or the 2D degenerate electron gas, which will be the subject of forthcoming works in the model.

Acknowledgments

This work was funded by Research Project No SA44/90 of the Consejería de Educación y Cultura de la Junta de Castilla y León and Research Project No PB 97-1331 of the DGESIC.

References

[1] Lee T H 1998 *The Design of CMOS Radio-Frequency Integrated Circuits* (Cambridge: Cambridge University Press)
[2] Chan Y J, Huang C H, Weng C C and Liew B K 1998 *IEEE Trans. Microw. Theory Tech.* **46** 611
[3] Shaeffer D K and Lee T H 1997 *IEEE J. Solid-State Circuits* **32** 745
[4] Tsividis Y P 1999 *Operation and Modeling of the MOS Transistor* (Boston: McGraw-Hill)
[5] Jindal R P 1986 *IEEE Trans. Electron Devices* **33** 1395
[6] Abidi A A 1986 *IEEE Trans. Electron Devices* **33** 1801
[7] Jacoboni C and Lugli P 1989 *The Monte Carlo Method for Semiconductor Device Simulation* (Berlin: Springer)
[8] González T, Pardo D, Varani L and Reggiani L 1995 *IEEE Trans. Electron Devices* **42** 991
[9] Martín M J, Pérez S, Pardo D and González T 2001 Monte Carlo analysis of the noise behavior in Si BJTs and SiGe HBTs at RF frequencies *J. Appl. Phys.* **90** 1582
[10] Mateos J, González T, Pardo D, Höel V and Cappy A 2000 *IEEE Trans. Electron Devices* **47** 1950
[11] Larson L E 1997 *RF and Microwave Circuit Design for Wireless Communications* (Boston, MA: Artech House Publishers)
[12] Mateos J, González T, Pardo D, Tadyszak P, Danneville F and Cappy A 1996 *Solid-State Electron.* **39** 1629
[13] Sung R, Bendix P and Das M B 1998 *IEEE Trans. Electron Devices* **45** 1769
[14] Laux S E and Fischetti M V 1988 *IEEE Electron Device Lett.* **9** 467
[15] Martín M J, Pardo D and Velázquez J E 2000 *Semicond. Sci. Technol.* **15** 277
[16] Martín M J, Velázquez J E and Pardo D 1996 *J. Appl. Phys.* **79** 6975
[17] González T and Pardo D 1996 *Solid-State Electron.* **39** 555
[18] Kim H, Min H S, Tang T W and Park Y J 1991 *Solid-State Electron.* **34** 1251
[19] Babiker S, Asenov A, Cameron N, Beaumont S P and Barker J R 1998 *IEEE Trans. Electron Devices* **45** 1644
[20] van der Ziel A 1986 *Noise in Solid State Devices and Circuits* (New York: Wiley)
[21] González T and Pardo D 1995 *IEEE Trans. Electron Devices* **42** 605
[22] Jen S H M, Enz C C, Pehlke D R, Schröter M and Sheu B J 1999 *IEEE Trans. Electron Devices* **46** 2217
[23] Berroth M and Bosch R 1990 *IEEE Trans. Microw. Theory Tech.* **38** 891
[24] Mateos J, González T, Pardo D, Tadyszak P, Danneville F and Cappy A 1998 *Solid-State Electron.* **42** 79
[25] Pucel R A, Haus H A and Stanz H 1974 *Adv. Electron. Electron Phys.* **38** 195
[26] Danneville F, Happy H, Dambrine G, Belquin J M and Cappy A 1994 *IEEE Trans. Electron Devices* **41** 779
[27] Goo J S, Choi C H, Danneville F, Morifuji E, Momose H S, Yu Z, Iwai H, Lee T H and Dutton R W 2000 *IEEE Trans. Electron Devices* **47** 2410
[28] Rothe H and Dahlke W 1956 *Proc. IRE* **44** 811
[29] Cappy A, Vanoverschelde A, Schortgen M, Versnaeyen C and Salmer G 1985 *IEEE Trans. Electron Devices* **32** 2787
[30] Greaves S D and Unwin R T 1993 *Microw. Opt. Techol. Lett.* **6** 60
[31] Dambrine G, Raskin J P, Danneville F, Vanhoenacker-Janvier D, Colinge J P and Cappy A 1999 *IEEE Trans. Electron Devices* **46** 1733
[32] Chen C H and Deen M J 1998 *Solid-State Electron.* **42** 2069