Ballistic nanodevices: a new concept in electronic design

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Abstract

When approaching the 10 nm gate length, the traditional downscaling of classic transistors does not provide an improvement of the device performance obstructed by the influence of parasitics and the appearance of short channel effects. We propose a new kind of devices based on the ballistic motion of electrons with two main goals, to increase the operation frequency and to improve the functionalities of classic devices. Since the aim of this novel concept is the replacement (or improvement) of the present day electronic devices, the room temperature operation is mandatory. High mobility materials (with room temperature mean free path around 100 nm) and modern electronic lithographic techniques allow the development of such kind of devices. In this paper, we present the fabrication, simulation and characterization of different types of ballistic nanodevices.

Samenvatting

Bij het naderen van de lengte van de 10 nm poort verstrekt traditionele downscaling van klassieke transistors geen verbetering van de componentenprestaties door de invloed van parasieten en de verschijning van korte kanaal- effekten. Wij stellen een nieuwe soort component voor, gebaseerd op de ballistische beweging van elektronen met twee belangrijke doelstellingen: de werkingsfrequentie te verhogen en de functionaliteit van klassieke componenten te verbeteren. Aangezien het doel van dit nieuwe concept de vervanging (of verbetering) van de hedendaagse elektronische componenten is, is kamertemperatuurwerking verplicht. Hoge mobiliteitsmaterialen (met kamertemperatuur betekent dit vrije baan rond 100 nm) en moderne elektronische lithografische technieken staan de ontwikkeling van dergelijk soort componenten toe. In dit artikel, stellen wij de vervaardiging, de simulatie en de karakterisering van verschillende soorten ballistische nanocomponenten voor.

Résumé

En approchant des longueurs de «grille» de 10 nm, la réduction des longueurs de grilles des transistors classiques ne fournit pas une amélioration des prestations des composants du fait de l'influence des parasites et l'apparition des effets de canal court. Nous présentons un nouveau genre de composants basés sur le mouvement balistique des électrons avec deux buts principaux, augmenter la fréquence de fonctionnement et améliorer les fonctionnalités des composants classiques. Puisque le but de ce concept innovant est le remplacement (ou l'amélioration) des dispositifs électroniques actuels, le fonctionnement à température ambiante est obligatoire. Les matériaux à mobilité élevée (avec un chemin libre moyen d'environ 100 nm à température ambiante) et les techniques lithographiques électroniques modernes permettent le développement d'un tel type de composant. Dans cet article, nous présentons la fabrication, la simulation et la caractérisation de différents types de nanocomposants balistiques.

Introduction

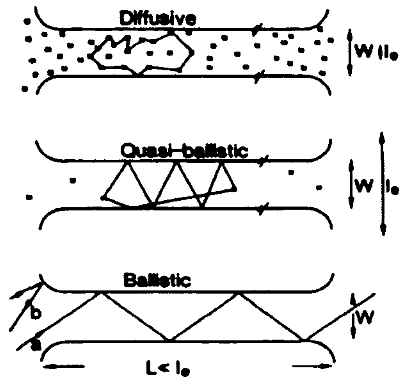
Because of the increasing amount of information to be processed and transmitted in modern electronic applications, the development of digital/analog electronic devices for data processing at ultra-high bit rates and/or on high frequency carriers is a hot subject of research. In classical semiconductor devices, the motion of electrons is diffusive (i.e. electrons are scattered by interactions with crystal atoms, electrons...), but, when the active area of a device is smaller than the electronic mean free path (the average distance an electron travels before it is scattered), electrons are only diffused by the walls of the device (Fig. 1). Electronic transport becomes ballistic and leads to novel macroscopic effects. Since 2000, it was demonstrated [1] that devices based on ballistic transport could operate even at room temperature in some semiconductor materials. In this paper we will explain the advantages of the ballistic devices, present the new effects that they provide and give some details of the fabrication, simulation and characterization of some of these novel structures.

Backround: material system

In order to realize ballistic devices working at room temperature, we have to choose a material system not only with long mean free path but also providing high carrier concentration in order to reduce the resistance of the devices and avoid important parasitic effects. Our devices are based on the GaInAs/AlInAs heterostructure on InP substrate shown in Fig. 2. The GaInAs channel is grown onto an AlInAs buffer, and, on the top of it, the undoped AlInAs barrier (including a thin layer of impurities, called δ-doped plane, supplying the conducting electrons) and the doped InGaAs cap layer (in order to provide good ohmic contacts) are fabricated. The main advantage of this kind of layer structure is that the doping layer is separated from the high mobility channel where the electrons flow, leading to high carrier concentrations and high mobility due to the absence of impurity scattering in the undoped InGaAs channel. The electrons are confined in the GaInAs channel due to the heterojunction with AlInAs, which imposes an energy barrier of about 0.5 eV that electrons cannot easily overcome. An Indium content of 70 % in the GaInAs channel is used in order to improve this energy barrier and also obtain higher electron mobility and longer mean free path. This kind of heterostructure has already been used for HEMTs (High Electron Mobility Transistors). Thus, this choice presents the advantage of technological compatibility with HEMTs. The thicknesses of the different layers were optimized in order to achieve the best compromise between high carrier density and long mean free path. In particular the thickness of the region separating the d-doped plane from the channel (called «spacer») was increased in order to reduce coulombian interactions. We have checked that the mean free path in the channel of such heterostructure is larger than 100 nm at room temperature. [2] We should then observe ballistic or quasi-ballistic effects for devices with active areas of less than 200 nm.

Fabrication of nano-devices

The fabrication of ballistic devices involves the realization of devices with a size of few tens of nanometers.



- *Device dimensions bigger than mean-free path l_e*
- *Device dimensions of order of mean-free path l_e*
- *Device dimensions smaller than mean free path l_e*

Fig. 1: Schematic illustration of electron motion versus device dimensions: W is the width of the channel, L its length

Fig. 2: Cross Section of the InAlAs/InGaAs epilayer on InP Substrate

Cap Layer	$Ga_{0.47}In_{0.53}As$	100 Å
Schottky	$Al_{0.48}In_{0.52}As$	150 Å
δ-doped	Si	4-4,5.10^{12}
Spacer	AlInAs NID	
Channel	$Ga_{0.3}In_{0.7}As$	150 Å
Buffer	$Al_{0.48}In_{0.52}As$ NID	2000 Å
Substrate	InP	

Several approaches exist in nanotechnology: some use a classical way, i.e. classical semiconductor processes (also called «top-down»), some use AFM manipulation or self-assembly (also called «bottom-up»)... In our case, we follow the top-down approach since the technology for this material system, which is close to a HEMT heterostructure, is quite mature, and, moreover, even if the dimensions are about 10000 times smaller than a hair, our devices are typically 30 times larger than carbon nanotubes.

As explained in the previous section, our devices are based on GaInAs/AlInAs heterostructure on InP substrate. Technological steps are then very similar to those used for a classical HEMT, i.e. the devices are fabricated as following: mesa etching to define the active region (see Fig. 3), ohmic contact formation and finally bonding pads.

For the realization of such devices, not only the precision of the lithographic step is important, also the achievement of a low-damage process on transport properties is a key issue. We will now focus on these step. To design the mesas, we used a high resolution negative resist called HSQ (Hydrogen-SilsesQuioxane) and an e-beam machine (LEICA EBPG5000+). The

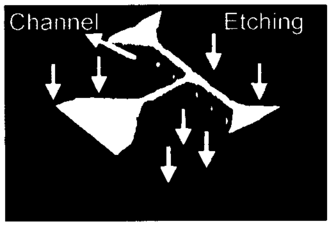


Fig 3: AFM picture of a T-Branch Junction

Fig. 4: SEM of a T-Branch Junction using wet etching process

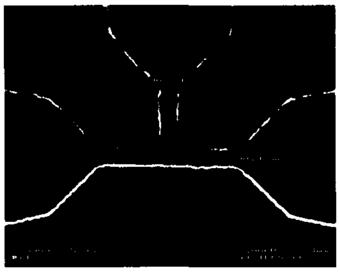


Fig. 5: SEM of a T-Branch Junction using dry etching process

minimum resolution of this tool is 7 nm. We have tested two ways for defining the geometry of the devices, one using wet etching and one using reactive ion etching ($CH_4/H_2/Ar$), RIE, shown in Figs. 4 and 5 respectively.

In order to optimize the realization of ballistic devices at room temperature several key parameters of both technologies were compared: edge roughness, etching undercut (i.e etching under the mask's edges) and depletion width at the interface between air and semiconductor. The summary of the comparison of these parameters is presented in Table 1.

Roughness for RIE is clearly better than for wet etching. The depletion width, W_d, due to surface charges at the interface air/semiconductor (that can be enlarged by the degradation of the surface due to etching process) was determined by using measurements of resistances of different channels. We found W_d of about 40 nm for both wet and dry etching at room temperature. The last important point is the etching undercut. For RIE, the measured dimensions of the fabricated devices are quite close to the mask dimensions, but for wet etching, undercut W_u is about 60 nm for an etching of about 80 nm. The minimum device size (see Fig 6.) that we are able to fabricate to get an non zero width of active area is then $2 \times (W_d + W_u)$. So, for RIE, the minimum device width is 80 nm ± 10 nm and for wet etching 200 nm ± 10 nm. We have therefore concluded that the best etching technology for the fabrication of ballistic devices is the Reactive Ion Etching (RIE).

Table 1: Etching comparison

$T = 300\,K$	RIE	Wet Etching
Edges	Low Roughness	High Roughness
Etching Undercut, W_u	Measured dimensions close to mask dimensions	> 60 nm
Depletion Width, W_d	40 nm ± 10 nm	40 nm ± 10 nm
Minimum Conductive Channel	80 nm ±10 nm	200 nm ± 10 nm

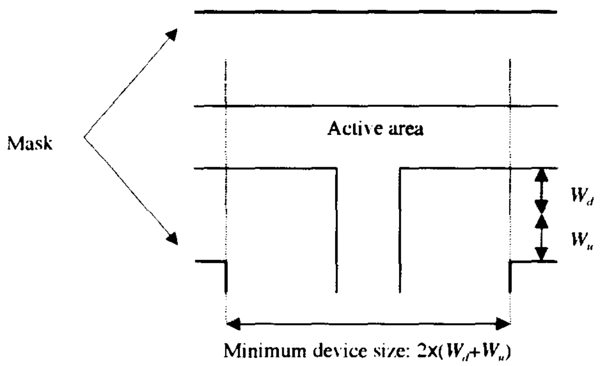


Fig. 6: Minimum device size

Simulation tool: Monte Carlo model

In order to understand the physical origin of the behaviour of the ballistic nano-devices, we have performed computer simulations making use of a semi-classical Monte Carlo model self-consistently coupled with a 2D Poisson solver. Monte Carlo (MC) simulations provide the solution of the Boltzmann equation by means of the microscopic representation in the time domain of the motion of the electrons within the devices, thus accounting for of their individual free flights and scattering mechanisms. Our model treats the electrons in a billiard ball-like manner (classical), but it locally takes into account the effect of degeneracy by using the rejection technique[3] (the scattering mechanisms are rejected when the final energy state is likely to be occupied). Even if quantum effects such as energy quantization (leading to 2D or even 1D transport) can be important when reducing the size of the devices, our study is focused on room temperature operation. Under these conditions, the considerable amount of thermal energy of the electrons (as compared with the quantized energy level steps) is enough to cancel the quantum effects which may appear at low temperatures. The surface charges appearing on the semiconductors in contact with the dielectrics are also considered in the model[4]. The origin of this negative surface charge, σ, are the electrons trapped at the surface states generated near the center of the bandgap of the semiconductor due to the break of the periodic crystalline potential (that provides the bulk semiconductor band profiles). The validity of this approach has been checked in previous works by means of the comparison with experimental results of AlInAs/GaInAs HEMTs[5] and different types of ballistic nanodevices[6]. Since contact injection is a critical point when dealing with ballistic transport, the velocity distribution and time statistics of injected carriers will be accurately modeled[7], characterized by a constant injection rate associated with the concentration at the contacts n_c.

For the correct modelling of these devices a 3D simulation would be necessary in order to take into account the effect of the lateral surface charges and the real geometry of the structure. However if some simplifications are made 2D simulations are enough to model the operation of these devices. Two kinds of 2D simulations can be made, front-view (FV) and top-view (TV), both sketched in Fig. 7. Within the FV simulations the layer structure will be taken into account, but the device in the z dimension is considered to be homogeneous. This kind of simulations will be useful for simple structures, like homogeneous channels, and will provide the concentration of carriers in each layer. On the other hand, to account for the top geometry of more complicated devices TV simulations will be made. They are made on the xy plane and therefore the real layer structure is not included and only the channel will be simulated (all the results shown in this paper are obtained from TV MC simulations).

Ballistic nanodevices

One of the most interesting characteristic of ballistics devices is observed in ballistic Three-Branch Junctions (called TBJs or YBJs, depending on the T or Y shaped geometry). Considering a symmetric T-shaped device, when biasing in push-pull fashion the left and right branches, $V = V_L = -V_R$, for diffusive structures a zero potential is expected to be found in the central branch, V_C, due to the identical resistances of the left and right branches. In the ballistic case, surprisingly, a negative value is found at the central branch. The representation of the experimental set-up, the SEM image of a real TBJ and the results for T-shaped TBJs with lengths of 980, 450, and 330 nm and 65 nm wide branches are shown in Fig. 5.

The Monte Carlo simulations of the TBJs have shown that the negative values of V_C appear due to the non homogeneity of the electron concentration in the horizontal branches, and thus the different resistance of the left and right branches. This happens due to (i) the depletion generated by the surface charges and (ii) ballistic transport. The surface charge lowers the electric potential when moving away from the contacts provoking the progressive depletion of the channel, thus leading to the typical minimum of potential and concentration in the middle of the structure, characteristic of space charge limited conditions[7] (Fig. 9). When the TBJ is biased, the concentration shows an asymmetric shape (higher near the negative electrode due to the electron ballistic motion) leading to a shift of the potential minimum towards the negative electrode. As a consequence, the potential at the center of the longitudinal channel is always negative (increasing with larger V) and propagates to the bottom of the vertical branch, thus leading to the characteristic bell-shaped values of V_C.

As stated in Ref. 8, this property of the TBJs can be very useful from a practical point of view, since it can be exploited to perform logical operations. It is clear, for example, that if we use left and right branches as inputs, the central branch output will perform the logic AND operation (V_c has high voltage, only when both V_L and V_R are high, low voltage in other case). With an adequate geometry, more complicated logic functions have already been implemented, for example a half adder[9]. Other possible applications of TBJs are those associated with their rectification capability (negative V_c, for positive and negative V) with the advantage of having very high cutoff frequencies. The use of TBJs as AC to DC power converters (THz detectors), or analog frequency doublers (due to the parabolic shape of the V_c vs. V characteristic), can also become an interesting field of application (see Fig. 10).

In order to optimize the performance of these applications, the amplitude of the

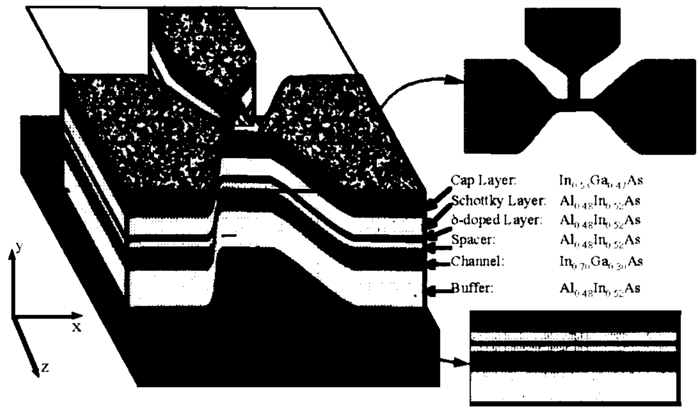


Fig. 7: Geometry and layer structure of the ballistic channels, and scheme of the 2D front-view (FV) and top view (TV) MC simulations

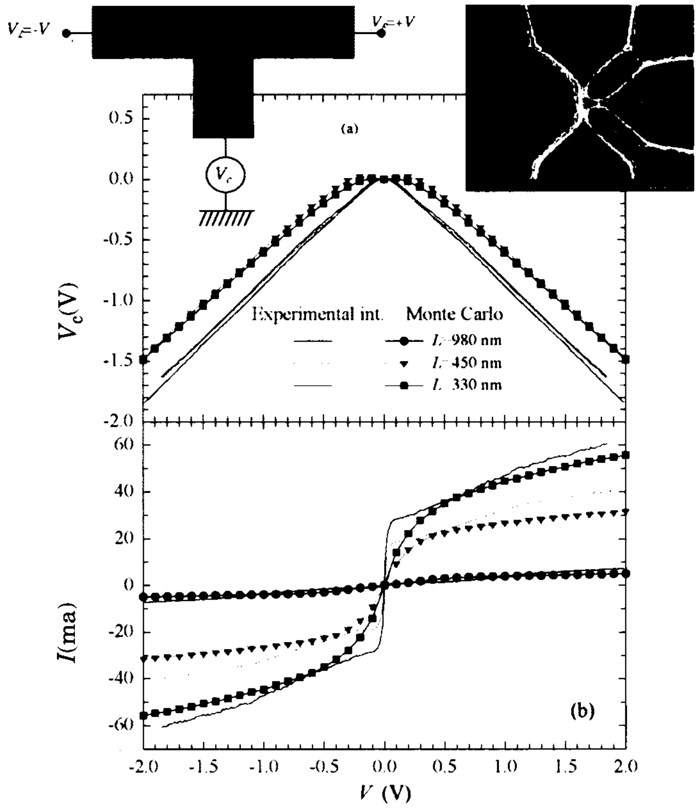


Fig 8: (a) V_C as a function of the intrinsic applied voltage, and (b) current flowing through the horizontal branches, I, when biasing in push-pull fashion $V = V_L = -V_R$ the T-shaped TBJs with lengths of 980, 450, and 330 nm and 65 nm wide branches. The results obtained from the Monte Carlo simulations of devices with the same geometries are also shown (lines with symbols). The representation of the experimental measurement setup and the SEM picture of one of the fabricated TBJs (with L = 330 nm) are shown at the top.

V_c vs. V curve should be increased as much as possible. For this sake the geometry of the T-shaped TBJs must be optimized reducing their length (so that the transport is almost purely ballistic) and narrowing the branches (enhancing the space charge effects). However, this second way of improvement greatly increases the impedance of the devices (to the range of KΩ) so that even very small parasitic capacitances (of the order of fF) prevent the extrinsic cutoff frequencies of the devices reaching the THz range. Therefore, other ways of improvement must be used, for example the use of Y-branch shaped junctions, that inject electrons into the central branch (thus making V_c more negative) and the use of more than one device in parallel[10]. By using these design guidelines and reducing the device parasitics, in Ref. 10 the operation of a double Y-branch junction as high frequency detector up to more than 40 GHz has already been demonstrated.

However, one of the problems for the ultra-high frequency operation of TBJs is the need for a push-pull bias (and the implementation of a reference terminal by means of an input microwave circuit). In order to avoid these problems, a new design for a ballistic rectifier was proposed in Ref. 11, by inserting a triangular scatterer (antidot) into the centre of a ballistic cross junction. With this geometry, while the voltage found at the top branch, V_T, is similar to those previously observed in T-shaped TBJs (due to the small carrier penetration into the top branch), the stronger injection of carriers into the bottom branch (because of the asymmetric geometry of the obstacle) enhances the curvature of the potential at this branch, V_B, thus providing negative output values, $V_{BT} = V_B - V_T$, and working as a classical diode bridge (as shown in the inset). In Fig. 11, we plot the values obtained for V_{BT} in the MC simulations of the device shown in the inset. The unequal penetration of carriers into the top and bottom branches due to the asymmetric geometry of the obstacle is therefore at the origin of the rectifying effect.

In order to demonstrate the intrinsic capability of this device for rectification at extremely high frequencies, the V_{BT} response to periodic AC signals with amplitude of 0.2 V and frequencies of 200 GHz, 1.0 THz and 2.0 THz applied

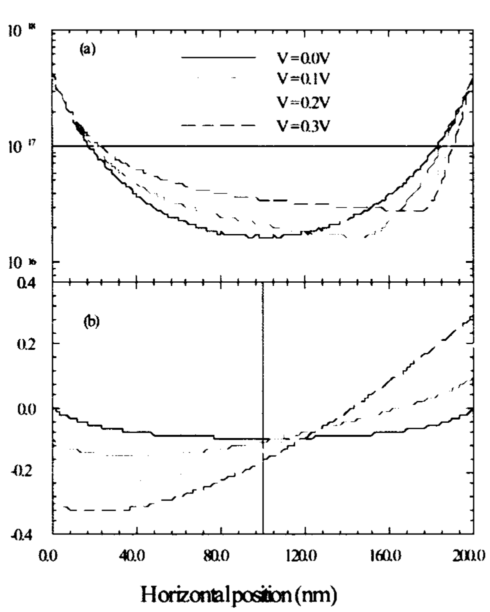


Fig. 9: (a) Electron concentration and (b) electric potential profiles along the middle of the horizontal branch of a TBJ with 50 nm wide and 75 nm long branches for different bias conditions ($V = V_L = -V_R$)

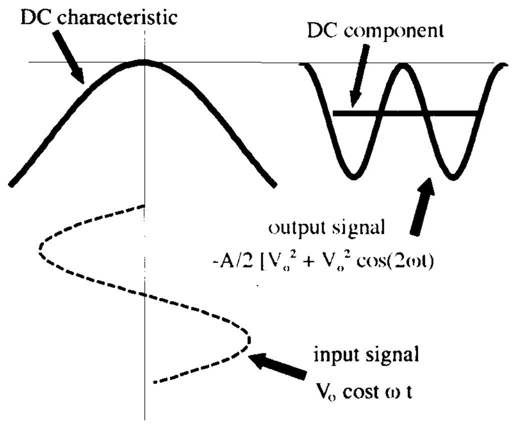


Fig. 10: Illustration of Detection and frequency doubling of RF signals

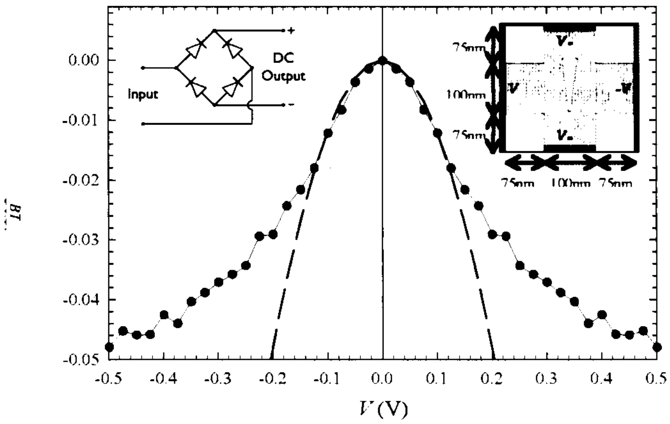


Fig 11: V_{BT} as a function of V when biasing with $V = V_L = -V_R$ the ballistic rectifier with the geometry shown in the inset. In this case, the result is the same if the potential is applied in push-fix fashion, $V_L = 0$ and $V_R = V$, thus avoiding the need for a reference voltage.

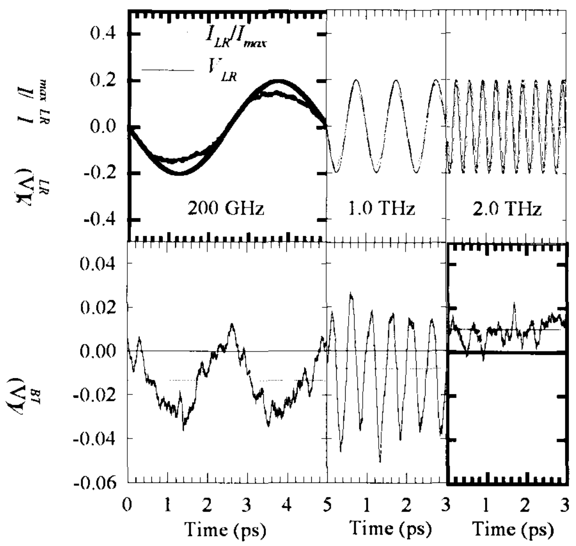


Fig. 12: V_{BT} response to periodic signals with amplitude of 0.2 V and frequencies of 200 GHz, 1 THz and 2 THz applied to V_{LR} (potential difference between left and right electrodes) in the ballistic rectifier of Fig. 9.

between left and right electrodes are plotted in Fig. 12. The excellent performance as frequency doubler or power detector in the THz range (at least up to 1 THz) is illustrated in the figure. Moreover, by reducing the size and optimizing the geometry of the device, its intrinsic cutoff frequency, sensitivity and linearity could be further improved. However, as in the case of TBJs, the influence of the parasitic capacitances together with the high impedance of the device, reduce the real cutoff frequency, so that strong efforts must be oriented to the reduction of the extrinsic capacitances.

Conclusion

In this paper we have presented some practical applications of ballistic transport together with the technological process and characterisation of room temperature ballistic devices, which confirm its feasibility. The behaviour of theses devices has been explained by using a semi-classical MC simulator, which has also been used to optimize their performances and to understand their limitations. Particularly, despite that THz intrinsic cut-off frequencies are expected for ballistic devices, the real performance of a single device is still far below the THz range due to the prevalence of parasitic effects (even with some optimizations of the design). In fact this conclusion could be extended to a large variety of nano-devices (including semiconductor nanowires or carbon nanotubes[12]): in order to improve the frequency performances of the devices the reduction of the parasitic effects is mandatory and a high level of parallelisation is needed.

Acknowledgements

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