Electronic Transport in Laterally Asymmetric Channel MOSFET for RF Analog Applications

Raúl Rengel and María Jesús Martín

***Abstract*—In this paper, an ensemble Monte Carlo investigation of the static and dynamic performances in the high-frequency domain of laterally asymmetric channel (LAC) bulk metal–oxide-semiconductor field-effect transistors (MOSFETs) is presented. A detailed comparison with a homogeneously doped bulk device is also included. The results presented show that the use of an asymmetric doping within the channel enhances nonequilibrium features as velocity overshoot, thus significantly improving the transconductance of the device. The gradual variation of doping is also responsible for a modification of the electrostatic conditions and the inversion charge profiles, provoking the reduction of the gate-to-source capacitance, a minor influence of surface scattering, reduced transit times, and higher mean free paths. A noticeable enhancement (as compared to a conventional device) in the RF and microwave frequency range of the dynamic performance of the transistors is also evidenced. This is mainly due to a better transconductance-to-current ratio, Early voltage, and open-loop gain, which are the results of the improvement of the charge transport conditions in the device at a microscopic level. Therefore, LAC MOSFETs can be a viable option to enhance the figures of merit of bulk silicon technology for high-frequency analog applications.**

***Index Terms*—Cutoff frequency, Early voltage, electronic transport, laterally asymmetric channel (LAC) metal–oxide-semiconductor field-effect transistor (MOSFET), Monte Carlo simulation, RF performance, transconductance.**

I. Introduction

SILICON devices and, in particular, metal–oxide-semiconductor field-effect transistors (MOSFETs) have been known to have an amazing development in the last decades. The continuous effort of researchers and engineers, guided by the scaling specifications of the International Technology Roadmap for Semiconductors [1], has boosted the RF performance of CMOS technology, thus making it a competitive contender for the design of cheap low-power low-voltage analog applications [2]–[5].

Unfortunately, the scaling of MOS transistors in the decananometer range is accompanied by a series of small-size effects that may potentially limit the use of these devices for analog applications [6], [7]. In order to overcome some of those problems and to improve the dynamic and noise yield of silicon MOSFETs, some authors have proposed the use of channel doping engineering as a feasible way to extend the RF performance of such devices and be competitive with III–V technologies in this frequency range [8]–[11]. In particular, several works have dealt with the investigation of the so-called laterally asymmetric channel (LAC) MOSFETs: In the fabrication process of a LAC MOSFET, a tilted angle implantation from the source side is carried out after the gate contact is formed. In this way, a progressively varying channel doping profile is obtained, with high doping values from the source to moderate or low doping values close to the drain [9], [12]–[14].

In order to fully understand the effect of an asymmetrical channel doping profile on the device performance, it is necessary to go beyond the values of the main static and dynamic figures of merit relevant to circuit designers and to focus on its relation to the microscopic transport properties. To achieve this goal, the Monte Carlo method applied to the simulation of semiconductor devices [15], [16] is one of the most appropriate tools. In this paper, we have used our in-house Monte Carlo 2-D simulator to carry out a physical modeling of charge transport. From the data obtained, an in-depth analysis of the static and dynamic performances of LAC MOSFETs is performed, including its comparison to symmetrically doped (SYM) transistors. Particular attention is paid to physical quantities such as channel transit times, average time between scatterings, mean free paths, etc., together with the longitudinal profiles along the channel (extracted from 2-D simulation) of electron velocity, concentration and potential drop inside the channel, and its relation to dynamic figures of merit. This paper is organized as follows. In Section II, the main simulation details are described, including the description of the topology of the devices under study and several features of the Monte Carlo simulator. In Section III, the most relevant results of our work, including microscopic quantities and dynamic figures of merit, are shown, and the main discussion is carried out. Finally, the conclusions are presented.

II. Simulation Details

The simulated structure is shown in Fig. 1, together with the transfer characteristics for both devices at $V_{\rm DS} = 2.0$ V. Two different cases have been considered for the channel doping. For the first simulated structure (LAC MOSFET), a steplike function is taken into account in order to reproduce the variation of a realistic Gaussian doping profile given by 2-D ISE-DESSIS (see Fig. 1) [8]. The maximum doping value is equal to $5 \cdot 10^{18}$ cm^{-3} close to the source and gradually decreases down to 10^{16} cm^{-3} at the drain end of the channel. In the case of a SYM MOSFET and in order to keep the same threshold voltage

Manuscript received March 1, 2010; revised May 28, 2010; accepted June 23, 2010. Date of publication August 3, 2010; date of current version September 22, 2010. This work was supported in part by the Ministerio de Ciencia e Innovación under Project TEC2009-07597, by the Consejería de Educación de la Junta de Castilla y León under Project SA010A07, and by the Fundación Samuel Solórzano Barruso under Project FS/21-2009. The review of this paper was arranged by Editor J. Woo.

The authors are with the Department of Applied Physics, University of Salamanca, 37008 Salamanca, Spain (e-mail: raulr@usal.es).

Digital Object Identifier 10.1109/TED.2010.2056290

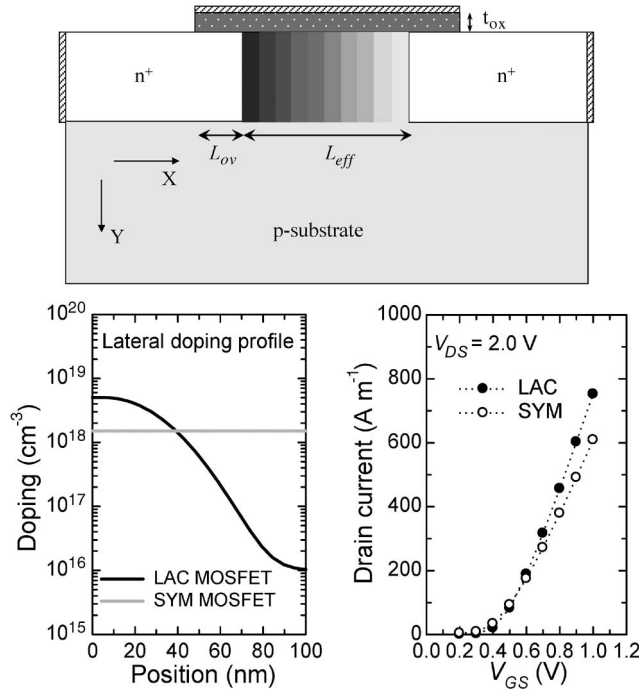

Fig. 1. Schematics of the simulated structures, including the doping profile for the LAC MOSFET and the transfer I–V curves for both devices. The origin for the X-coordinate (longitudinal) is the beginning of the channel close to the source, and the origin for the Y-coordinate (transversal) is considered to be the Si–SiO_2 interface.

as for the case of the LAC device, a uniform doping equal to $1.5 \cdot 10^{18}$ cm^{-3} is taken into account. Such consideration for the doping profiles for LAC and SYM transistors has also been proposed by other authors [8]. The effective gate length $L_{\rm eff}$ is 100 nm, the oxide thickness $t_{\rm ox}$ is 1.8 nm, the overlap length $L_{\rm ov}$ is considered to be 15 nm, and the depth of the source and drain regions is equal to 30 nm.

The results presented in this paper have been obtained by means of our 2-D Monte Carlo device simulator, which main details can be found in [17] and [18] and references therein. Impurity scattering, acoustical and optical phonon scattering, and surface scattering are included in the simulations. The simulator has been successfully tested with experimental measurements for several types of MOSFET devices [17], [18]. Although the simulator provides the 2-D results for the main internal quantities (electron concentration, energy, velocity, etc.), to provide a clearer discussion and comparison between simulated structures, it is more adequate to present the 1-D profiles of these quantities along the channel. In this way, the longitudinal 1-D profiles shown in the graphs are appropriately obtained, weighting the 2-D values by the carrier concentration along the vertical (y) axis. The procedure to obtain the 1-D average profiles is similar to that explained in [19]. As an example, to achieve the 1-D profiles for the average velocity, we use

$$\langle v_x(x)\rangle = \left(\int \bar{v}_x(x,y)\bar{n}(x,y)dy\right) \Big/ \int \bar{n}(x,y)dy).$$

From the relevant data related to the microscopic movement of carriers crossing the channel, it is possible to perform a complete study of electronic transport inside the device. In order to obtain the internal quantities related to electronic transport (mean free paths, transit times, number of scattering events, etc.), a counting region corresponding to the effective channel is considered [19], [20]. Each electron inside the counting region is flagged, and all the relevant data related to its movement are recorded (number and type of scattering events, free flight times, distance travelled in the X- and Y-axes, etc.). Simulations over a 100-ps simulation time are required in order to achieve the adequate statistical resolution (by letting a large number of superparticles to cross the channel) for the different bias points and devices considered. The dynamic figures of merit are obtained from the calculation of the four complex and frequency-dependent admittance (Y) parameters. These are given by the Fourier analysis of transient values of instantaneous currents recorded when small voltage steps are separately applied to terminals, as in [17].

III. Results and Discussion

In order to carry out a fair comparison between LAC and SYM transistors, identical drain current conditions $(I_D = 300\ \mu\text{A} \cdot \mu\text{m}^{-1})$ are considered in the longitudinal profiles shown here, which is well suited for the subsequent discussion about the dynamic performance of the devices. It has been pointed out by other authors that the appearance of nonequilibrium carrier transport (and, particularly, velocity overshoot) in short-channel devices opens the possibility of improving the transconductance and, hence, the dynamic performance of MOS transistors [21].

Fig. 2 shows the longitudinal (E_x) field, potential, and average electron velocity profiles for the LAC and SYM devices under identical current conditions at $V_{\rm DS} = 2.0$ V. The potential profile presents a larger slope for the LAC transistor in the first two-third of the channel, while the conventional MOSFET concentrates the potential variation at the vicinity of the drain n^+ region. This implies important differences in the electric field experienced by carriers crossing the conducting channel. As it can be observed, close to the drain in the LAC MOSFET, the negative peak value of E_x is equal to -716 kV $\cdot$ cm^{-1}, while it is much larger $(-1240$ kV $\cdot$ cm$^{-1})$ for the SYM MOSFET. On the contrary, in the middle part of the channel and close to the source, the longitudinal electric field is significantly more elevated for the asymmetrically doped transistor (about -100 kV $\cdot$ cm^{-1} at $x = 20$ nm) than for the SYM MOSFET (-20 kV $\cdot$ cm^{-1} at that same longitudinal location). The SYM device presents the typical velocity profile for a MOS transistor in saturation [22], with an important velocity overshoot close to the drain, while in the most part of the channel, the velocity values are below the saturation velocity in bulk silicon $(10^7$ cm $\cdot$ s$^{-1})$. However, in the case of the LAC MOSFET, the velocity increases much more rapidly from source to drain, thus presenting an overshoot mostly at the middle part of the channel: Indeed, with the Gaussian doping profile considered, the maximum velocity value (which is lower than the peak value in the SYM device) is obtained practically at the midpoint of the effective channel. From that point on, the longitudinal velocity tends to decrease in the LAC MOSFET. This is due to the combination of several factors: First of all, the population in

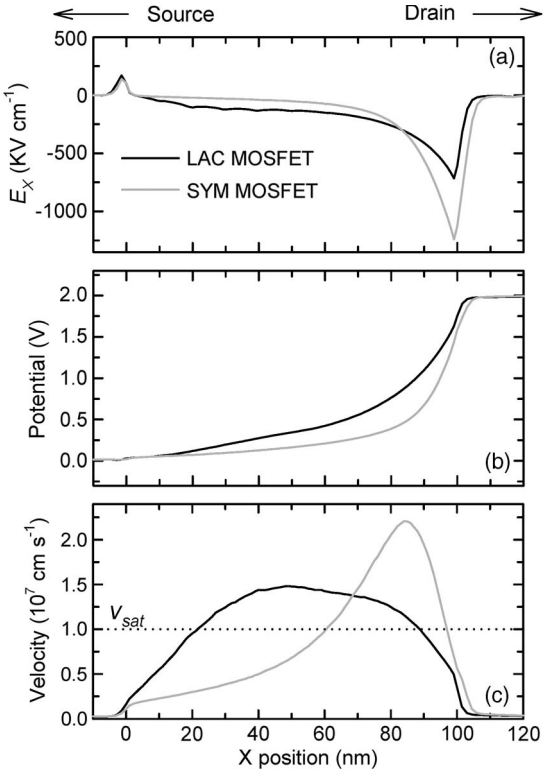

Fig. 2. (a) Longitudinal electric field, (b) potential profiles, and (c) average drift velocity in the X-axis at $I_D = 300\ \mu\text{A} \cdot \mu\text{m}^{-1}$ and $V_{\text{DS}} = 2.0$ V.

the X valleys of the conduction band is not uniform along the channel, as a consequence of the variation of the longitudinal and transversal electric fields. In the case of the LAC MOSFET, the profile of the vertical field (which will be discussed afterward) provokes a progressive increase in the population of [010] X valleys along the channel, thus augmenting the total population of X valleys transversal to the longitudinal field along the [100] direction and contributing to the initial increase of the average velocity due to their reduced effective mass. For the SYM MOSFET, this occurs closer to the drain. On the other hand, when the electrons reach energies on the order of hundreds of millielectronvolts, the average electron momentum tends to relax by the effect of isotropic phonon scattering, and the average velocity rapidly drops for the LAC MOSFET, while still high kinetic energies are observed in the last part of the channel. Consequently, significant nonequilibrium phenomena are observed.

The results shown for the different longitudinal profiles (potential, velocity, and E_x) are in a general good agreement with those presented by other authors [9], [21]. However, in order to fully understand the nature of transport within the channel of LAC MOSFETs, it is also extremely important to examine the vertical dimension, and in particular the electric field transversal to electronic transport, E_y, which is usually not discussed in the literature but, in this case, plays a key role. Fig. 3 shows the vertical electric field (E_y) profile along the channel for the LAC and SYM MOSFETs at $I_D = 300\ \mu\text{A} \cdot \mu\text{m}^{-1}$. While the peak value of E_y close to the source is practically identical (around 1000 kV $\cdot$ cm^{-1}) in both structures, in the middle part of the channel, the conventionally doped SYM

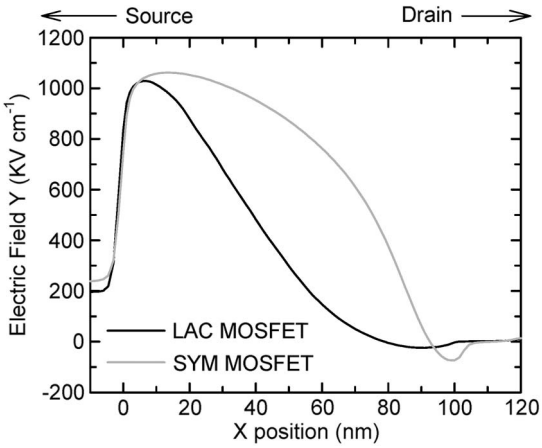

Fig. 3. Transversal electric field profiles at $I_D = 300\ \mu\text{A} \cdot \mu\text{m}^{-1}$ and $V_{\text{DS}} = 2.0$ V.

MOSFET presents much more elevated values than the LAC device. For example, at $x = 50$ nm, the electric field is equal to 300 kV $\cdot$ cm^{-1} for the LAC MOSFET, while in the SYM transistor, it practically triples this value, being E_y equal to 900 kV $\cdot$ cm^{-1}. This fact is consequence of the different action of a uniform gate voltage over the asymmetrically doped channel, since in a MOS junction, the vertical electric field inside the semiconductor depends on the square root of the local substrate doping: The lower the doping, the lower the vertical electric field. Therefore, in the LAC MOSFET, the vertical field is consequently strongly curtailed along the channel, and a minor influence of surface scattering is expected.

In Fig. 4, we present the average number of total isotropic scatterings, phonon scattering, and surface scatterings suffered by an electron travelling from source to drain, as a function of the drain current at $V_{\text{DS}} = 2.0$ V. As it can be observed, there are a much reduced number of the total isotropic scattering events in the LAC MOSFET. On the one hand, phonon scattering is much more relevant for the asymmetrically doped device. The high values of momentum reached by carriers crossing the channel yield an enhanced probability for those events to occur. As it can be observed, for low drain currents (i.e., low V_{GS}), the number of phonon scatterings in a LAC MOSFET almost doubles the number of phonon scatterings in a SYM device. As the gate voltage is increased and higher drain energies are reached, the differences tend to reduce, but even so, the number of phonon scatterings keeps larger in the LAC MOSFET. However, on the other hand, there is a paramount divergence in the number of surface scatterings under the gate, being much more elevated for the conventional device. This is due to the higher vertical electric field in the SYM MOSFET that enhances the pile-up of electrons against the Si–SiO_2 interface along the most part of the channel and therefore increases the number of surface scattering events. Consequently, the LAC MOSFET benefits, in an inherent manner, of a reduced influence of carrier interactions with the Si–SiO_2 interface, thus contributing to the boosting of velocity overshoot in the whole channel previously commented. This result suggest that, although a longitudinal doping variation is considered, there is also a very important modification of transport features along the vertical dimension,

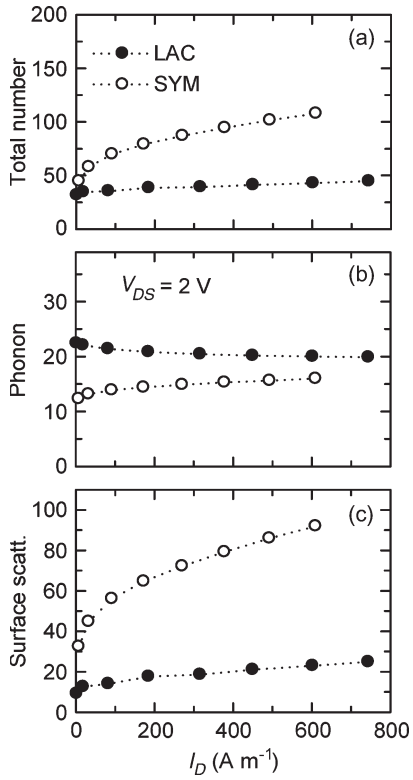

Fig. 4. (a) Average total number of isotropic scattering events, (b) phonon scattering, and (c) surface scatterings as a function of drain current at $V_{\rm DS} = 2.0$ V.

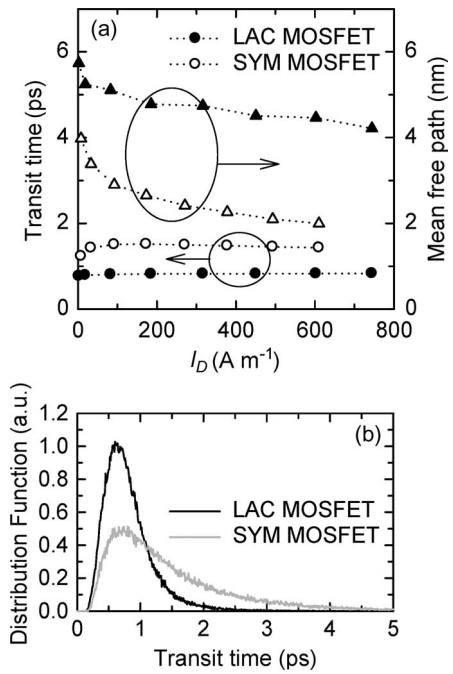

Fig. 5. (a) Average transit time (circles) and mean free path (triangles) as a function of drain current for $V_{\rm DS} = 2.0$ V and (b) transit time distribution function at $I_D = 300\ \mu\text{A} \cdot \mu\text{m}^{-1}$ and $V_{\rm DS} = 2.0$ V.

thus resulting in a 2-D effect on transport that indeed enhances the velocity overshoot in LAC MOSFETs.

If a complete picture of transport inside the device is desired, it becomes necessary to examine microscopic quantities related to the movement of carriers when crossing the channel. The combination of more favorable electrostatic conditions and reduced influence of surface scattering provokes much more reduced transit times of carriers in the LAC MOSFET, as it can be observed in Fig. 5(a). Electrons take practically half the time to cross the channel as compared to the conventional device. When examining the transit time distribution function [Fig. 5(b)] for $I_D = 300\ \mu\text{A} \cdot \mu\text{m}^{-1}$, a much more pronounced peak of the distribution for the LAC MOSFET can be observed, while the SYM device shows a smoother profile consequence of the larger dispersion in the transit time values in this case. Both graphs evidence a closer-to-ballistic behavior in the laterally asymmetrically doped device as compared to the conventional device. The mean free path [Fig. 5(a)] is subsequently much larger in the asymmetrically doped transistor.

Such improvement in the electronic transport conditions inside the channel is also translated into a better dynamic performance of the transistors in the RF and microwave range. Fig. 6(a) shows the total gate capacitance C_g (computed as $C_{\rm gs} + C_{\rm gd}$) and the transconductance g_m as a function of the drain current in the high frequency range (both parameters remain constant in the RF and microwave range, up to at least 80 GHz). As it can be observed, lower and higher values of C_g and g_m, respectively, are obtained for the asymmetrically doped transistor, which presents an intrinsic transconductance

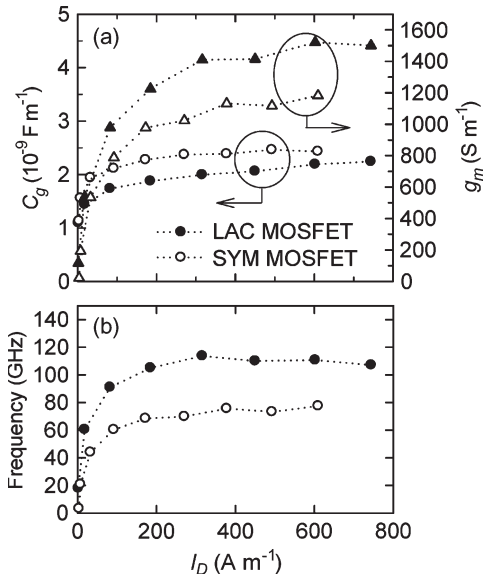

Fig. 6. (a) Gate capacitance and transconductance in the RF and microwave range and (b) cutoff frequency of current gain as a function of drain current for $V_{\rm DS} = 2.0$ V.

equal to 1410 S m^{-1} for the bias point providing the highest cutoff frequency. The reduced capacitive coupling with the gate is related to the minor influence of the vertical electric field over the channel charge in this case, as previously discussed; in the LAC MOSFET, charge is not so strongly tied under the gate oxide as in the SYM device. The Gaussian doping profile, on the contrary, favors the travelling of electronic charge across the channel and, consequently, the increase of drain current. When examining the longitudinal profiles of the electron concentration and velocity for several values of $V_{\rm GS}$ (not shown in the graphs), it can be observed that, for the LAC

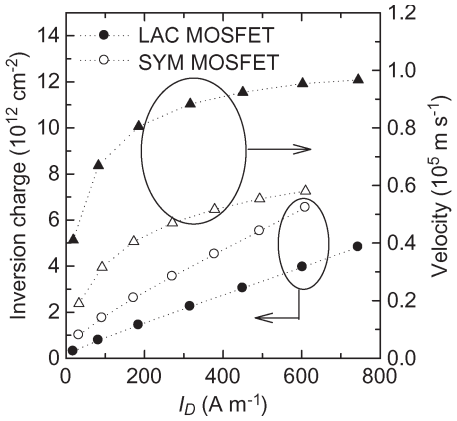

Fig. 7. (Circles) Average electron concentration and (triangles) velocity in the channel as a function of drain current for $V_{\rm DS} = 2.0$ V.

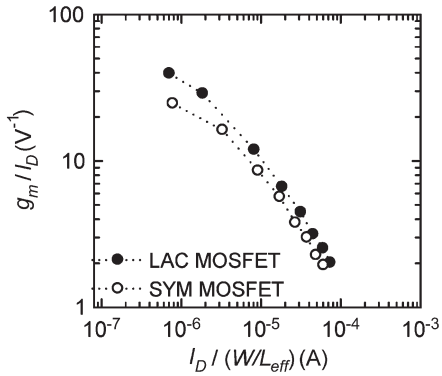

Fig. 8. Transconductance-to-current ratio as a function of the normalized drain current for $V_{\rm DS} = 2.0$ V.

MOSFET, there exists a reduced variation of inversion charge as $V_{\rm GS}$ is raised under constant $V_{\rm DS}$ conditions, which explains the reduced values of the gate-to-source capacitance $C_{\rm gs}$ and, hence, the total gate capacitance C_g. This is due to the higher doping values in the channel close to the source as compared to the constant value of the conventional device. Consequently, the gate potential is less effective in order to increase the channel inversion charge close to the source. Fig. 7 shows the average electron concentration and velocity in the whole channel. As it can be observed, the lower values of inversion charge in the LAC device are compensated by a much higher average velocity, thus providing the higher current values previously mentioned. Moreover, in order to investigate the origin of the higher transconductance found in the LAC device, one may pay attention to the values of concentration, velocity, and the increase of both quantities when $V_{\rm GS}$ is augmented. In this way, the transconductance has three main components, i.e., increase of concentration times the velocity $(\Delta n \times v)$, increase of velocity times the concentration $(\Delta v \times n)$, and the third coming from the product of both increases $(\Delta n \times \Delta v)$. Computing these values from the data obtained in the Monte Carlo simulation, it has been found that the first component $(\Delta n \times v)$ is the most important for both devices, particularly for the LAC MOSFET (in which up to 90% of g_m is due to this contribution for the largest $V_{\rm GS}$ values). Therefore, the main reason of the enhanced transconductance in the asymmetrically doped device is the much higher velocity values and, particularly, the elevated speeds reached by electrons in the middle part of the channel.

The lower gate-to-source capacitance values and the higher transconductance have the direct consequence of a much elevated current gain cutoff frequency (f_T) for the LAC MOSFET as compared to the conventional device [Fig. 6(b)]. The cutoff frequencies shown here are obtained by extrapolation of the current gain to the unity value directly computed from the admittance parameters and agree well with the usual expression for this figure of merit in terms of g_m and C_g [23]. As it can be observed, the highest f_T's are reached for drain currents between 350 and 400 S m^{-1}, with a maximum value equal to 113.5 GHz for the LAC MOSFET and 75 GHz for the SYM MOSFET, which means an outstanding improvement, as high as +50%.

In the design of low-power analog applications, the transconductance-to-current ratio (g_m/I_D) of the transistor is a key figure of merit. It indicates the efficiency of the transistor in using current to achieve a given value of g_m [24]; in other words, it has been defined as a quality factor, the transconductance representing the amplification delivered by the device and the current indicating the power dissipated to obtain that amplification [25]. Moreover, it is used by designers to determine the width and length of the device to obtain the performance required in a certain application. Fig. 8 shows the transconductance-to-current ratio as a function of the normalized drain current for the two transistors under study. As it can be observed, the LAC MOSFET clearly outperforms the conventional device for all the currents considered (which correspond to moderate and strong inversion conditions). While the ratio tends to drop in strong inversion for both devices, the relative improvement provided by the LAC device is still very significant, although the main differences are observed in moderate inversion; in particular, in the moderate inversion regime, the values reached are close to the ideal weak inversion value 38.6 V^{-1} (considering a body factor equal to 1) [26]. It must be reminded that the results presented correspond to the intrinsic performance of the transistors and do not include the effect of fringing capacitances or contact resistances.

The LAC MOSFET also presents higher values of the Early voltage $(V_{\rm EA})$ as compared to the conventional device. The Early voltage values are extracted from the ratio of the drain current I_D and the output conductance $g_{\rm ds}$. The results for both transistors are shown in Fig. 9(a). The improved Early voltage values obtained for the LAC MOSFET are due to a much reduced output conductance: We have checked that, while the variation of the drain voltage shows little influence on the channel charge in both transistors, in the case of the SYM MOSFET, there is an important increase of the carrier velocity close to the drain (not shown in the graphs) when a drain voltage step is applied. Such velocity increase, which does not take place in the LAC MOSFET, is the main responsible for the higher $g_{\rm ds}$ values observed in the SYM MOSFET and, hence, the lower values of $V_{\rm EA}$ in strong saturation conditions. In the moderate inversion regime, the Early voltage values tend to be similar (and low) in LAC and SYM devices. Such reduction in the Early voltage values close to weak inversion has also

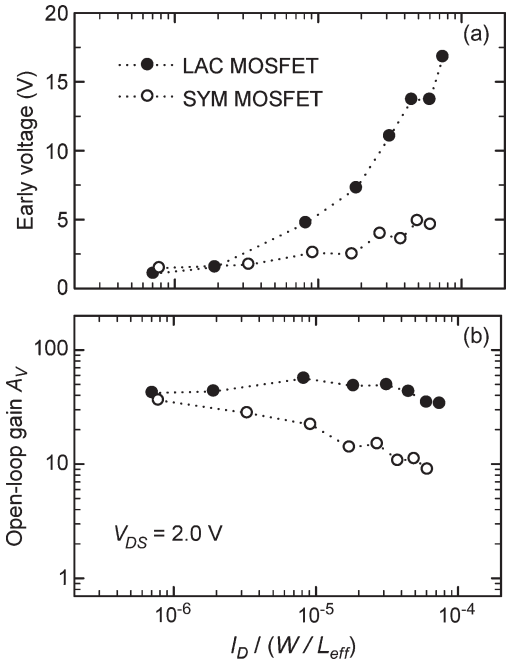

Fig. 9. (a) Early voltage and (b) open-loop gain as a function of the normalized drain current for $V_{\rm DS} = 2.0$ V.

been observed by other authors in multichannel and UTB SOI MOSFETs [27].

The transconductance-to-current ratio and the Early voltage combine to provide a much better open-loop gain for the asymmetrically doped device [Fig. 9(b)], particularly in the strong inversion regime. The results are consistent with those observed by other authors in the case of graded-channel SOI devices [24], in which the channel doping does not vary smoothly as in the case of a LAC transistor, but there is a sharp variation in the channel doping.

Therefore, it can be concluded that the use of an asymmetric doping in the channel (which, on the other hand, introduces a relatively more elaborated fabrication process) yields higher transconductance efficiency for RF analog design and an improved open-loop gain, thus enhancing the performance of bulk MOS technology for analog applications. The noise performance of LAC MOSFETs will be the subject of a forthcoming paper.

IV. Conclusion

A Monte Carlo investigation of the electron transport properties and high-frequency dynamic performance of LAC bulk MOSFET has been presented. Results have shown a preeminence of velocity overshoot in the whole channel in LAC MOSFETs, extremely favored by improved electrostatic conditions as compared to a conventionally doped device. In particular, the strong reduction of the vertical electric field in a wide part of the channel significantly shrinks the influence of surface Si–SiO_2 interactions, thus enhancing ballistic movement features inside the channel, which is reflected in a much larger mean free path and a sharper transit time distribution function. The improvement in the electronic transport conditions echoes into a much better RF and microwave dynamic performance. An outstanding improvement in the cutoff frequency is obtained, owing to a reduced gate-to-source capacitance and a larger transconductance. Moreover, higher values of the Early voltage and better transconductance-to-current ratio and open-loop gain are obtained due to the more favorable transport conditions. Results demonstrate the feasibility of LACs as a way to significantly improve the dynamic performance of conventional bulk MOSFETs.

Acknowledgment

The authors would like to thank Dr. T. C. Lim and Prof. F. Danneville for the helpful discussions and the suggestions for defining the simulated structure.

References

[1] The International Technology Roadmap for Semiconductors, San Jose, CA, 2007. [Online]. Available: http://public.itrs.net

[2] L. E. Larson, "Silicon technology tradeoffs for radio-frequency/mixed signal systems-on-a-chip," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 683–699, Mar. 2003.

[3] V. Kilchytska, A. Neve, L. Vancaillie, D. Levacq, S. Adriaensen, H. van Meer, K. De Meyer, C. Raynaud, M. Dehan, J.-P. Raskin, and D. Flandre, "Influence of device engineering on the analog and RF performances of SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 577–588, Mar. 2003.

[4] V. Dimitrov, J. B. Heng, K. Timp, O. Dimauro, R. Chan, J. Feng, W. Hafez, T. Sorsch, W. Mansfield, J. Miner, A. Kornblit, F. Klemens, J. Bower, R. Cirelli, E. Ferry, A. Taylor, M. Feng, and G. Timp, "High performance sub-50 nm MOSFETs for mixed signal applications," in *IEDM Tech. Dig.*, 2006, pp. 213–216.

[5] F. Schwierz and C. Schippel, "Performance trends of Si-based RF transistors," *Microelectron. Reliab.*, vol. 47, no. 2/3, pp. 384–390, Feb./Mar. 2007.

[6] C. Fiegna, "The effect of scaling on the performance of small signal MOS amplifiers," in *Proc. ISCAS*, May 2000, pp. 733–736.

[7] D. Buss, "Device issues in the integration of analog/RF functions in deep sub-micron digital CMOS," in *IEDM Tech. Dig.*, Dec. 1999, pp. 423–426.

[8] T. C. Lim, R. Valentin, G. Dambrine, and F. Danneville, "MOSFETs RF noise optimization via channel engineering," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 118–121, Jan. 2008.

[9] K. Narasimhulu, M. P. Desai, S. G. Narendra, and V. Ramgopal Rao, "The effect of LAC doping on deep submicrometer transistor capacitances and its influence on device RF performance," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1416–1423, Sep. 2004.

[10] M. A. Pavanello, J. A. Martino, V. Dessard, and D. Flandre, "Analog performance and application of graded-channel fully depleted SOI MOSFETs," *Solid State Electron.*, vol. 44, no. 7, pp. 1219–1222, Jul. 2000.

[11] H. V. Deshpande, B. Cheng, and J. C. S. Woo, "Channel engineering for analog device design in deep submicron CMOS technology for system-on-chip applications," *IEEE Electron Device Lett.*, vol. 49, no. 9, pp. 1558–1565, Sep. 2002.

[12] J. P. John, V. Ilderem, C. Park, J. Teplik, K. Klein, and S. Cheng, "A low voltage graded-channel MOSFET (LV-GCMOS) for sub 1-V microcontroller application," in *VLSI Symp. Tech. Dig.*, Jun. 1996, pp. 178–179.

[13] S. Mahapatra, V. Ramgopal Rao, C. D. Parikh, J. Vasi, B. Cheng, and J. C. S. Woo, "A study of 100 nm channel length asymmetric channel MOSFET by using charge pumping," *Microelectron. Eng.*, vol. 48, no. 1–4, pp. 193–196, Sep. 1999.

[14] P. Sarkar, A. Mallik, and C. K. Sarkar, "Study on the performance of sub 100 nm LACLATI MOSFETs for digital application," *Microelectron. Reliab.*, vol. 49, no. 4, pp. 392–396, Apr. 2009.

[15] C. Jacoboni and P. Lugli, *The Monte Carlo Method for Semiconductor Device Simulation*. Vienna, Austria: McGraw-Hill, 1989.

[16] C. Moglestue, *Monte Carlo Simulation of Semiconductor Devices*. London, U.K.: Chapman & Hall, 1993.

[17] R. Rengel, M. J. Martín, G. Dambrine, and F. Danneville, "A Monte Carlo investigation of the RF performance of partially-depleted SOI MOSFETs," *Semicond. Sci. Technol.*, vol. 21, no. 3, pp. 273–278, Mar. 2006.
[18] R. Rengel, M. J. Martin, T. Gonzalez, J. Mateos, D. Pardo, G. Dambrine, J.-P. Raskin, and F. Danneville, "A microscopic interpretation of the RF noise performance of fabricated FDSOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 3, pp. 523–532, Mar. 2006.
[19] J. Lusakowski, M. J. M. Martínez, R. Rengel, T. González, R. Tauk, Y. M. Meziani, W. Knap, F. Boeuf, and T. Skotnicki, "Quasiballistic transport in nanometer Si metal-oxide-semiconductor field-effect transistors: Experimental and Monte Carlo analysis," *J. Appl. Phys.*, vol. 101, no. 11, p. 114 511, Jun. 2007.
[20] J. S. Martin, A. Bournel, and P. Dollfus, "On the ballistic transport in nanometer-scaled DG MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 7, pp. 1148–1155, Jul. 2004.
[21] S. Odanaka and A. Hiroki, "Potential design and transport property of 0.1-μm MOSFET with asymmetric channel profile," *IEEE Trans. Electron Devices*, vol. 44, no. 4, pp. 595–600, Apr. 1997.
[22] S. E. Laux and M. V. Fischetti, "Monte-Carlo simulation of submicrometer Si n-MOSFETs at 77 and 300 K," *IEEE Electron Device Lett.*, vol. 9, no. 9, pp. 467–469, Sep. 1988.
[23] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. New York: McGraw-Hill, 1999.
[24] M. Galeti, M. A. Pavanello, and J. A. Martino, "Evaluation of graded-channel SOI MOSFET operation at high temperatures," *Microelectron. J.*, vol. 37, no. 7, pp. 601–607, Jul. 2006.
[25] K. Rajendran and G. S. Samudra, "Modelling of transconductance-to-current ratio (g_m/I_D) analysis on double-gate SOI MOSFETs," *Semicond. Sci. Technol.*, vol. 15, no. 2, pp. 139–144, Feb. 2000.
[26] J.-P. Colinge, "Fully-depleted SOI CMOS for analog applications," *IEEE Trans. Electron Devices*, vol. 45, no. 5, pp. 1010–1016, May 1998.
[27] T. C. Lim, E. Bernard, O. Rozeau, T. Ernst, B. Guillaumot, N. Vulliet, C. Buj-Dufournet, M. Paccaud, S. Lepilliet, G. Dambrine, and F. Danneville, "Analog/RF performance of multichannel SOI MOSFET," *IEEE Trans. Electron Devices*, vol. 56, no. 7, pp. 1473–1482, Jul. 2009.

Raúl Rengel was born in Tarrasa, Spain, in 1974. He received the B.S. and Ph.D. degrees in physics from the University of Salamanca, Salamanca, Spain, in 1997 and 2003, respectively.

From 1998 to 2000, he was with the Electronics Group, Department of Applied Physics, University of Salamanca, as a grant holder, where he became an Assistant Professor in 2001. In 2004, he was a Postdoctoral Researcher with the Institute d'Electronique, de Microélectronique et de Nanotechnologies, Villeneuve d'Ascq, France. Since 2007, he has been an Associate Professor with the University of Salamanca. His main research activity is the Monte Carlo modeling of electron transport in silicon devices, including the investigation of electronic noise processes and small-signal behavior in the high-frequency range in SOI MOSFET transistors and nonconventional silicon devices.

María Jesús Martín was born in Salamanca, Spain, in 1969. She received the B.S. and Ph.D. degrees in physics from the University of Salamanca, Salamanca, in 1992 and 1996, respectively.

Since 1992, she has been with the Electronics Group, Department of Applied Physics, University of Salamanca, as a grant holder. Her graduate work focused on the simulation of transport and electronic noise in bipolar Si and SiGe structures. In 1995, she became an Assistant Professor. In 1997 and 1998, she was with the Electronic Components Technology and Materials, Technological University of Delft, Delft, The Netherlands. Since 2002, she has been an Associate Professor with the University of Salamanca. Her current research interest is in the field of Monte Carlo modeling of electronic transport, dynamic characterization, and noise in the RF range of submicrometer silicon devices, with particular focus in scaling issues and the performance of nonconventional MOSFETs.