Design and Analysis of High Performance Ballistic Nanodevice-Based Sequential Circuits Using Monte Carlo and Verilog AMS Simulations

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***Abstract*— In this paper, we propose a design of traditional sequential circuits using high performance Ballistic Deflection Transistor (BDT). BDT technology was developed and experimentally proven to operate at Terahertz frequencies. Different structures of BDTs have been developed successfully to realize combinational logic functionality. Monte Carlo (MC) simulations have been extensively used to study these structures. By taking into account the effect of surface charges and dielectrics, we are able to correctly reproduce the non-linear I-V transfer characteristics, to predict scaling down behavior and to estimate the very high switching speed. We then used a three parameter Gaussian peak as a predictive model for the BDT and integrated it with Verilog AMS module to confirm the functionality of the designed circuits. Finally, we used a recently developed level-sensitive D-latch using two-BDTs structure, to explore traditional sequential circuits such as Shift Registers (SRs), Frequency Divider and Johnson Ring Counter, which play a pivotal role in many processing systems as common datapath operators. The simulation results have indicated the correct logic functionality of the implemented sequential circuits.**

***Index Terms*— Ballistic Deflection Transistors (BDT), D-Flip Flop, D-Latch, frequency dividers, Monte Carlo simulations, sequential circuits, shift registers, Verilog AMS.**

I. Introduction

With the aggressive scaling in CMOS devices, the semiconductor industry has seen a tremendous growth during the past thirty years. As the CMOS scaling is near its limit, the industry aims for new/alternative devices to complement conventional silicon devices [1]. On the other hand, extreme rises in global Internet traffic lead to great demand for high performance data processing and storage systems. Thus an emerging device that can operate data systems at Terahertz (THz) frequencies will presumably impact the world's economy enormously. At the beginning of this decade, the new emerging devices were classified into three different classes namely Electrically Dependent Nanodevices (ballistic, tunneling or electrostatic transport), Magnetically Dependent Nanodevices (magneto static or spin transport) and Mechanically Dependent Nanodevices (restructuring physical), based on the physical phenomena behind their operation [2]. Currently, ferroelectric devices, piezoelectronic and orbitronic devices have also joined the group of emerging devices [3]. Table I indicates list of few emerging devices and their acronyms that are considered by Nanoelectronics Research Initiative (NRI) and various research centers [3]. Each of these centers is focused on developing benchmarking circuits to compare the performance of emerging devices [4].

TABLE I
List of Few Emerging Devices Considered by Various Research Centers [3]

Device	Acronym	Device	Acronym
Si MOSFET high performance	CMOS HP	Si MOSFET low voltage	CMOS LV
van der Walls FET	vdWFET	Homojunction III-V TFET	HomJTFET
Graphene nanoribbon TFET	gnrFTET	Interlayer tunneling FET	ITFET
GaN TFET	GaNFET	Graphene pn-junction	GpnJ
Ferroelectric FET	FEFET	Negative capacitance FET	NCFET
Piezoelectric FET	PiezoFET	Bilayer pseudospin FET	BisFET
Excitonic FET	EXFET	Metal-insulator transistor	MITFET
SpinFET	SpinFET	All-spin logic	ASL
Charge-spin logic	CSL	Spin torque domain wall	STT/DW
Spin majority gate	SMG	Spin torque oscillator	STO
Spin wave device	SWD	Nanomagnetic logic	NML

[The cell color designates the computational variable: blue=electronic, orange =ferroelectric, yellow=straintronic, purple=orbitronic, red=spintronic devices]

Among the above mentioned emerging devices, electronic devices have better switching speeds compared to other devices, but have both higher active and standby power [3]. Ferroelectric and Magnetoelectric devices have significantly lower active power, but have their own switching speed limitations [3]. Although these devices have successfully implemented sequential circuits, the quest for device suitable for high performance energy efficient computing is still on.

Ballistic devices are one among electrically dependent devices that have potential to succeed CMOS in several

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application areas because of their ability to operate at THz frequencies [2]. A novel six terminal transistor, namely Ballistic Deflection Transistor (BDT), which is based on the properties of a ballistic transport [5]–[7], has been intentionally developed to operate at very high speed with low power consumption [8]–[10]. During the past decade, a significant research has been done with this structure [11]–[17]. A single BDT, when properly biased can act as a logic gate [18]. A NAND gate and GPG BDT structure have been developed to realize the combinational logic circuits and had been successfully demonstrated [19], [20]. This present work focuses on developing sequential circuits, using BDT based D-latch that was proposed recently using Verilog AMS model [21], and analyzing their functional logic [22]. Simulations play a key role in a development of logic circuits based on these emerging devices.

The paper is further organized as follows: Section II provides the background of ballistic devices and Ballistic Deflection Transistors. Section III describes Monte Carlos (MC) simulations. Section IV discusses the predictive model of the BDT and its integration to Verilog AMS model. Section V discusses the details of circuit design. This section explains the importance of voltage at drain terminals and the optimization for values of resistors in the BDT circuits. Section VI briefly explains the recently proposed D-latch and D Flip-Flop (DFF) using BDTs and also estimates their delay with respect to different sizes. Section VII consists of sequential circuits that are developed using BDT based DFF along with their simulation results.

II. Ballistic Deflection Transistors

A. Ballistic Deflection Transistor

The BDT is a six terminal coplanar structure etched into a heterostructure comprising a two dimensional electron gas (2DEG) layer. The high mobility III-V compound allows electrons to travel with an estimated electron velocity of the order of 10^8 cm/s—more than 2.5× faster than electron transport in silicon. The device consists of a grounded electron source (SS), left and right gates (LG, RG), and three biased drains (TD, LD, RD) as shown in Fig.1.a. The side gates act like inputs and steer the electrons towards their respective output drain terminals. The top drain behaves like a constant pull-up potential used to accelerate the electrons from the source toward the central deflector. Nanometric dimensions and materials allow the electrons to travel in a quasi-ballistic manner at room temperature, guided by the deflector and lateral gate potentials.

The SEM image of a BDT, with a channel width (W) of 300 nm, is shown in Fig.1a. The low capacitance of the 2DEG features the results in an estimated cutoff frequency (f_T) in the terahertz range. It has been fabricated in an InGaAs/InAlAs heterostructure with an InP substrate, using mask layers defined by electron beam lithography, with reactive ion etching used to create the raised mesas [13].

B. BDT Operation

The measured response of the BDT at room temperature with a grounded source and 1 V bias applied to each of the three drains across a range of differential gate voltages

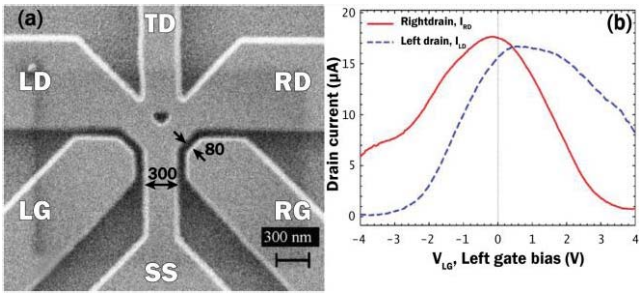


Fig. 1. (a) SEM image of BDT: Top Drain (TD), Right Gate (RG), Left Gate (LG), Right Drain (RD), Left Drain (LD) and Source (SS) with channel width 300 nm and trench of 80 nm. (b) Typical transfer characteristics of BDT (both are obtained [13]).

is shown in Fig. 1(b). The BDT is operated in push-pull configuration ($V_{LG} = -V_{RG}$). The asymmetry between the left and right outputs is caused by process variation and a slight offset in contact placement. A positive left gate and negative right gate voltage results in current gain through the left output branch; current gain is seen through the right output branch when the voltages are reversed. It was observed that drain current initially increases as a function of gate voltage and then decreases. This happens due to channel pinch off when gate voltage is high enough.

III. MC Simulations

The modelling of our device has been performed by an ensemble MC simulator self-consistently coupled with a 2D Poisson solver [11]. Electrons dynamic is accurately simulated using all necessary models in order to obtain a precise output current. As the nanometric size of the BDT increase the surface-volume ratio, a particular attention has been devoted to surface charges located at the interface semiconductor-dielectric. An appropriate model is used, allowing enough time to these surface charges to self-consistently adapt themselves with the surrounding carrier concentration. Calculation time is increased but precision is enhanced. More details can be found in [23].

Fig. 2 shows experimental left (I_{LD}) and right (I_{RD}) output drain currents in function of gate voltages (in push-pull configuration), which have been compared with our MC simulations. Result shows a remarkably good agreement with measurements. The magnitude of the current and the sharp drop at both sides of the maximum are correctly reproduced.

Previous calculations considering a fixed surface charge value everywhere were correct at equilibrium and enough as first approximation, but they were overestimating the current at high gate voltage and weren't able to closely follow the bell-shape characteristic [23]. Thus the self-consistent surface charge model is the only accurate one to perform reliable simulations in dc.

Investigation on very high speed performances has also been carried out. In order to evaluate the switching frequency of the BDT, and due to the complex non-linear nature of the device associated to the key role of surface charges, a special way has been used. Two long enough simulations are made on two symmetric polarizations in order to let the surface charge σ to stabilize. When the output current is correct, the two charge distributions ($\sigma 1$ and $\sigma 2$) are extracted. Then new simulations

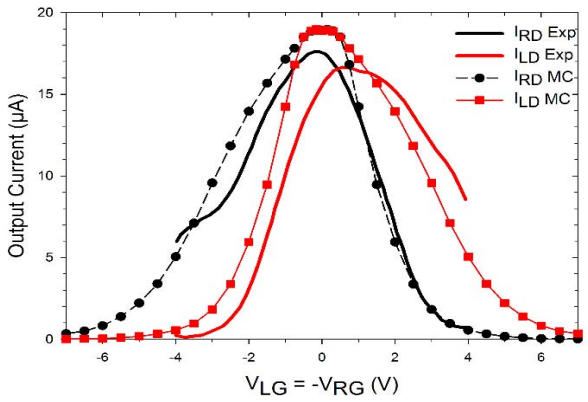


Fig. 2. Comparison of experimental and MC transfer characteristics.

are performed with a bias switching, implying two cases. In the first one, or model 1, the surface charge distribution changes, from $\sigma 1$ to $\sigma 2$, instantaneously with the bias, leading to an ideal case where the time constant is very short. In the second case, or model 2, surface charges aren't changing at all, implying a very long time constant. These two models are considered limits of real behavior, as very little is known about the velocity of increase or decrease of surface charges value.

Results are shown in Fig. 3, for two different size of our BDT device. The change of current level represents the switch of gate voltage from one value to its opposite (from -2 to 2 V), resulting to electrons to be steered from one drain to the other. Gate voltage configuration has been chosen for the biggest current level difference. The observed delay is in the order of 3 picoseconds for the 300 nm width channel device, providing a theoretical frequency of operation of about 300 GHz. In the case of the smaller device, 100 nm width channel, the time delay decrease to 1 ps, corresponding to a frequency of 1 THz. These results are confirming the outstanding performances of our device in the THz domain.

IV. BDT Analytical Model

A three parameter Gaussian peak analytical model of the BDT was initially developed to aid circuit design, provided by [24] and altered to (1),

$$I_d = a \times \exp\left(-K \times \left(\frac{V_{LG} \pm V_o}{b}\right)^2\right) \quad (1)$$

where I_d is the drain current and V_o is the gate voltage corresponding to the current peak. The parameter "a" is function of both channel width and drain applied bias V_{DD}, while "b" controls the width of the bell shape I-V curve and K depends on the applied permittivity.

The predictive analytical model has been updated using MATLAB to fit the transfer curves of smaller size BDTs with channel length of 100 nm, appropriately fitting MC results.

A. Effect of Dielectrics

The output characteristics (V_{LG} vs I_{RD}) of a smaller BDT with channel width of 100 nm and trench width of 27 nm, integrated with different dielectric materials is shown in Fig. 4. The relative permittivity value ε of dielectric materials used

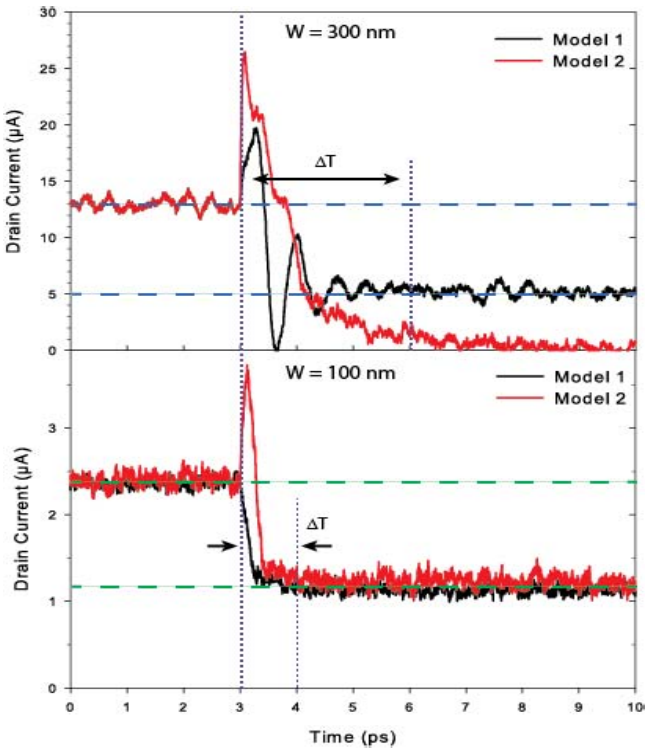


Fig. 3. MC estimations for different sizes of BDTs on switching level of drain currents w.r.t. change in gate voltages using two different models.

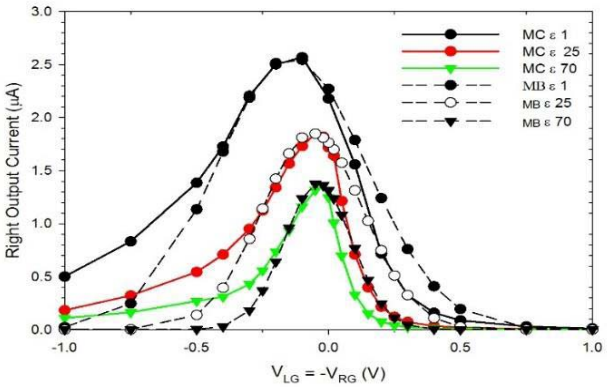


Fig. 4. Monte Carlo and MATLAB simulations for different permittivity

of air, Al_2O_3 and deionized (DI) water are 1, 27, and 70 respectively. The increase of permittivity improves the electrostatic gate control and reduces the pinch-off voltage. It is also enhancing the transconductance and increasing the ratio of output current to leakage current [25].

V. BDT Logic Circuit Design

In order to analyze sequential circuits developed using BDT logic structure, it is essential to analyze the circuit design of a single BDT. In the following simulations, BDT of channel width 100 nm and trench width 27 nm integrated with dielectric material Al_2O_3 is considered, as it has relatively better gate control and high Ion/Ioff ratio compared to BDTs of different size and dielectric material. BDTs can be operated at different configurations and are as follows:

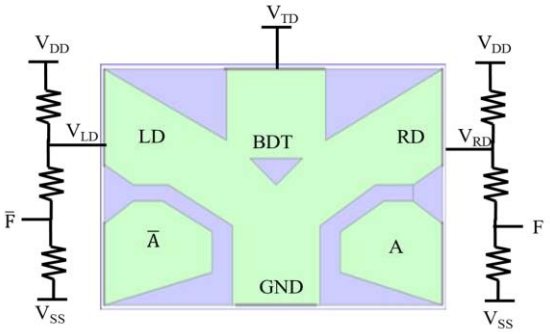


Fig. 5. Circuit design of single BDT whose side output drain terminals connected to string of resistors.

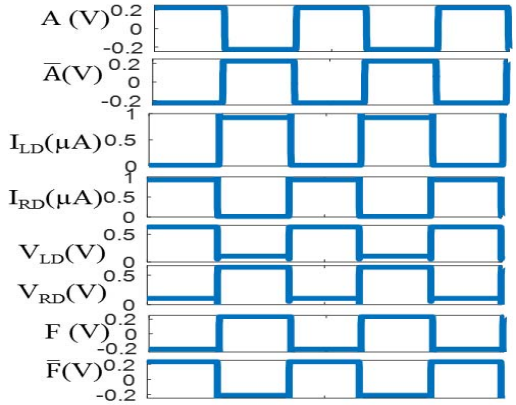


Fig. 6. Simulation results of single BDT circuit, acting like an Inverter.

A. Push-Pull Configuration

In this configuration, a BDT logic functionality is similar to dual-rail logic design; each BDT has complementary inputs and complementary outputs. Thus the circuit outputs can be used as both buffer and inverter. Fig. 5, shows inverter/buffer circuit design using single BDT. The side drain terminals of the BDT are connected to series of resistors between V_{DD} and V_{SS}, which act like current-to-voltage converters [9]. In this circuit, the A and $\overline{A}$ are connected to input gate terminals V_{RG} and V_{LG} respectively whereas I_{LD} and I_{RD} are the currents flowing through output drain terminals LD and RD respectively. However, the circuit output functions F and $\overline{F}$ are connected to BDT through string of resistors in such a way that the output current from drain terminals of BDT will affect their voltage values.

Simulation results of single BDT are shown in Fig. 6. It should be observed that when A/V_{RG} is high (225 mV), the I_{RD} is high (934 nA) and hence F is low (-212 mV). Similarly, when A/V_{RG} is low (-225 mV), the I_{RD} is low (13 nA) and hence F is high (234 mV). Thus the single BDT circuit acts like inverter and buffer.

In this case, it is vital to notice the voltage at right drain terminal V_{RD}. If V_{RD} is negative, the right drain terminal will not collect the electrons deflected into them and when the electrons do not flow into the right drain terminal, then the voltage value of F rises to logic high. Hence in order to obtain precise output voltage value at node F, values of resistors connected to drain terminals are to be accurately calculated such that voltage values at V_{LD} and V_{RD} are always maintained with least positive voltage that can always allow electrons into them. In this simulation, we found the least values of V_{LD} and V_{RD} to be 120 mV.

B. Push-Push/ Pull-Pull Configuration

Generally, BDTs are operated in push-pull configuration. However, they also operate in two other configurations namely, push-push/ pull-pull. A BDT is said to be operated in these configurations if same logic level is provided to both the input gates. If both the input gates are at logic low level, then the BDT is operated in push-push configuration and similarly if both the input gates are at logic high level, BDT is said to be in pull-pull configuration. In push-push configuration, the both the gate voltages will try to deflect electrons to the opposite drain terminals. However, if the magnitude of both inputs is high, say –225 mV for BDT of channel width 100 nm, the bottom branch will be pinched off. Thus, in this configuration there will be no current in drain terminals and hence both F and $\overline{F}$ are logic high state simultaneously. However, in pull-pull configuration, the electrons will be steered towards the side drain terminals and this allows both F and $\overline{F}$ to be in logic low state simultaneously. Table II indicates the operation of BDT at different configurations.

TABLE II
DIFFERENT KINDS OF BDT OPERATING CONFIGURATION

Configuration	V_{RG}	V_{LG}	I_{RD}	I_{LD}	F	$\overline{F}$
Push-Pull	A	$\overline{A}$	High	Low	Low	High
Push-Push	$\overline{A}$	$\overline{A}$	Low	Low	High	High
Pull-Pull	A	A	High	High	Low	Low

C. Current-to-Voltage Converters

For any emerging device, it is very important to drive logic of the next state from present state. In BDTs, this cannot be realized because the output from the drain terminals is flow of electrons and gate voltage is generally provided as inputs. Hence in order to drive next stage logic, the side drain terminals are connected to string of resistors that act like current-to-voltage converters. Significant amount of time has been devoted to find the value of resistors. We have recently proposed a memory latch with cascading logic of BDTs by using current-to-voltage converters [26].

VI. BDT D-LATCH AND D FLIP-FLOP DESIGN

A. D-Latch using BDT

The schematic diagram of D-latch developed using BDTs is shown in Fig.7. It consists of two BDTs namely BDT1 and BDT2 [21]. The top drain terminal of both BDTs are connected to V_{TD}. The source of BDT2 is connected to clock signal *Clk* and the source of BDT1 is connected to complementary clock signal $\overline{Clk}$. The data signals D and $\overline{D}$ ($\overline{D}$ is the complementary data signal) are provided to right and left gate terminals of BDT1 respectively and the output signals Q and $\overline{Q}$ are connected to right and left gate terminals of BDT2 respectively. The left drains (LD1 and LD2) and right drains (RD1 and RD2) of both BDTs are shorted and connected to string of resistors. These resistors act like a current-to-voltage converter that supports logic with BDTs.

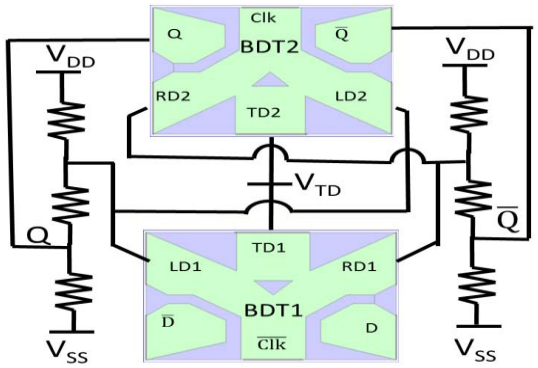


Fig. 7. D-Latch circuit design using Ballistic Deflection Transistors (BDTs).

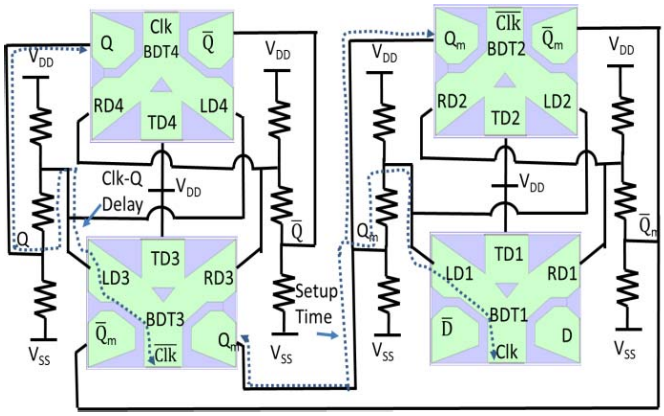


Fig. 8. D-FF circuit design with Clk to Q and setup time delay paths using Ballistic Deflection Transistors (BDTs)

The operating voltage range of D-latch depends on the value of resistors used in the circuit.

When *Clk* is in logic 1 state ($\overline{Clk}$ is logic 0, 0V), BDT2 will not have electron flow through its drain terminals because there exists no potential difference between V_{TD} and *Clk*. However, BDT1 will be functional because of the potential difference V_{TD} and $\overline{Clk}$. The electrons from source of BDT1 will be steered into LD1/RD1 by data signal *D* and $\overline{D}$. This makes *Q* to follow *D* and thus the D-latch is in transparent mode. When *Clk* is low, the electrons from source of BDT2 are steered to RD1/RD2 by output voltage *Q* and $\overline{Q}$. This makes *Q* to hold its previous state as well as makes it independent of data signal *D*. Since the output *Q* is dependent on the level of the clock signal, the D-latch is considered as *level-sensitive* D-latch.

B. D Flip-Flop Using BDT

The D Flip-Flop (DFF) developed using BDTs follow the concept of master-slave flip flop [22]. The circuit design of DFF shown in Fig. 8. is a combination of two D-latches, a positive level sensitive D-latch, comprising BDT3 and BDT4, acting as a slave and a negative level sensitive D-latch comprising BDT1 and BDT2, acting as a master. Since, the negative level-sensitive D-latch is followed by positive level-sensitive D-latch, the DFF a positive edge triggered DFF. Similarly, a negative edge triggered DFF can be realized when a positive level-sensitive D-latch is followed by a negative level-sensitive D-latch.

C. Simulation Results of D-Latch and DFF

The simulation results of both D-latch (negative level-sensitive D-latch) and DFF (positive edge triggered) are shown in Fig. 9. The master latch of the DFF is a negative level-sensitive D-latch comprising BDT1 and BDT2. The outputs of this latch Q_m and $\overline{Q}_m$ are intermediate outputs of the DFF and are simultaneously inputs to slave latch comprising BDT3 and BDT4.

They are explained as follows: When clock signal *Clk* is in logic 0 state (0 mV) and data signal *D* is changed, the intermediate outputs Q_m and $\overline{Q}_m$ will follow the data signal, allowing the master latch to be transparent mode. At the same time, slave latch will be in hold mode and its previous data will be retained. When clock signal Clk is transitioned from logic low (0 mV) to logic high (650 mV), slave latch

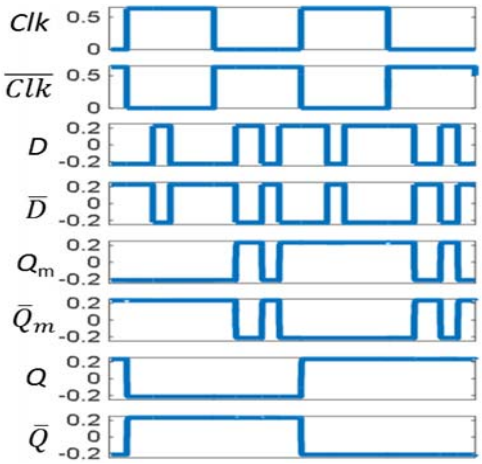


Fig. 9. Simulation results of BDT based D-Latch and DFF

TABLE III
TIMING PARAMETERS ESTIMATED FOR PROPOSED D-FF

Delay Parameters	Time	
	BDT_300nm	BDT_100nm
Clk to Q	«1ps	«1ps
D to Q	2ps to 3ps	<1ps
Setup time	2ps to 3ps	<1ps
Hold time	«1ps	«1ps
Clock Period	6ps	< 2ps

follows the master latch and the master latch holds its data. Thus, the output signals *Q* and $\overline{Q}$ stores the value of data signals *D* and $\overline{D}$ at positive edge of every clock signal *Clk* respectively. The logic low and logic high values of both data and output signals are -225 mV and +225 mV respectively.

D. Estimation of Delay

Table III shows analytically estimated delays of the BDT based DFF using MC simulations, which are mentioned in Section III of this paper. The D to Q delay in the worst case is estimated to 3ps and less than 1ps in DFF developed using BDT of channel width 300 nm and 100 nm respectively. The setup time will be similar to that of D to Q delay and hold

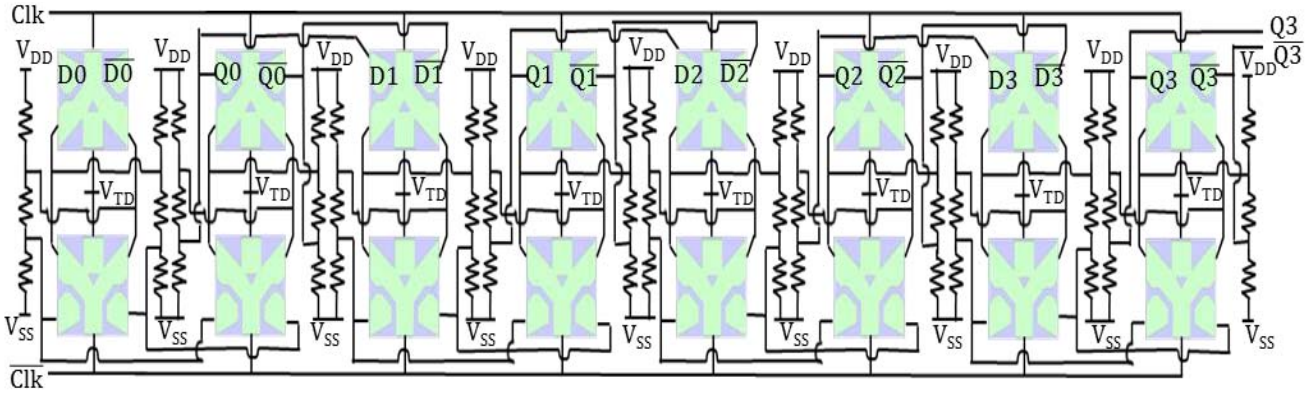


Fig. 10. 4-bit BDT DFF based SISO shift register

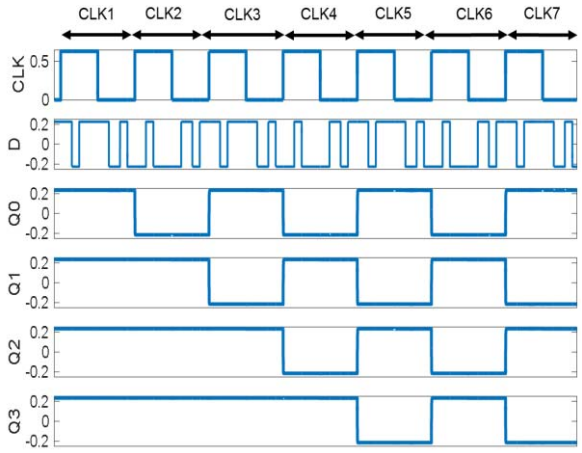


Fig. 11. Simulation results of 4-bit BDT DFF based SISO shift registers

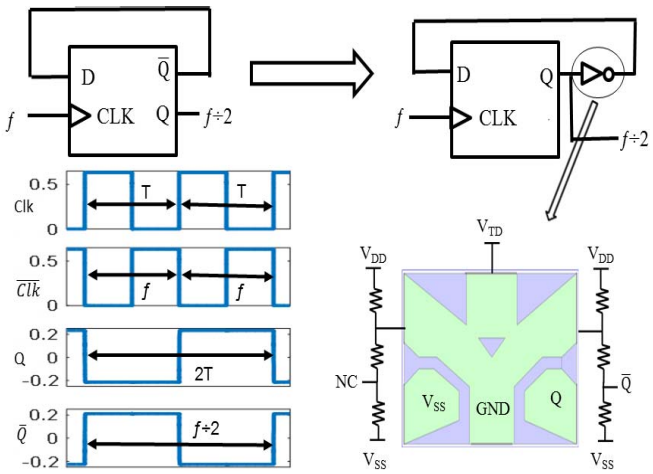


Fig. 12. BDT DFF based Divide-by-2 Circuit.

TABLE IV
LOGIC FUNCTIONALITY OF BDT BASED 4-bit SHIFT REGISTER

CLK	Q0	Q1	Q2	Q3
1	1	1	1	1
2	0	1	1	1
3	1	0	1	1
4	0	1	0	1
5	1	0	1	0
6	0	1	0	1
7	1	0	1	0

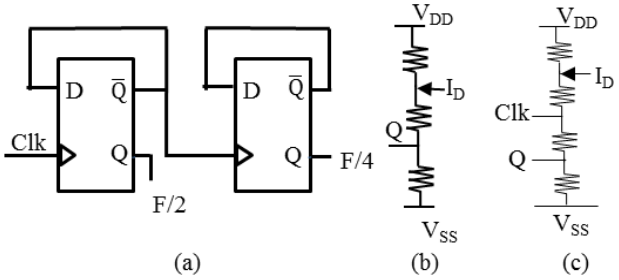


Fig. 13. (a) Divide by 2, 4; frequency divider circuit using DFF. (b) String of resistors connected to drain terminals of BDT, to act like current-to-voltage converters and have only one output voltage value (Q). (c) Similar to (b) but has two different output voltage values. (Clk and Q).

time will be similar to Clk to Q time, and will be very much less compared to setup time as the *Clk* signals are acting as source. On the whole, the clock period of the proposed DFF is estimated to be twice the setup time (considering the worst case, $T_H + T_{Clk\text{-}Q}$ equals T_S). Thus, the operating frequencies of proposed DFFs are expected to range from 200GHz to 500GHz depending on size of the BDTs.

$$T_P \geq T_S + T_H + T_{Clk\text{-}Q}$$
$$T_P \geq 2 * T_S$$

Where T_P is clock period, T_S is setup time, T_H is hold time, $T_{Clk\text{-}Q}$ is clock to Q delay. The result data are consistent with previously obtained experimental results on 1μ m BDTs which are reported in [17]. Also, with further optimization of the BDT device and interconnections, the proposed DFF should be able to operate at THz frequencies.

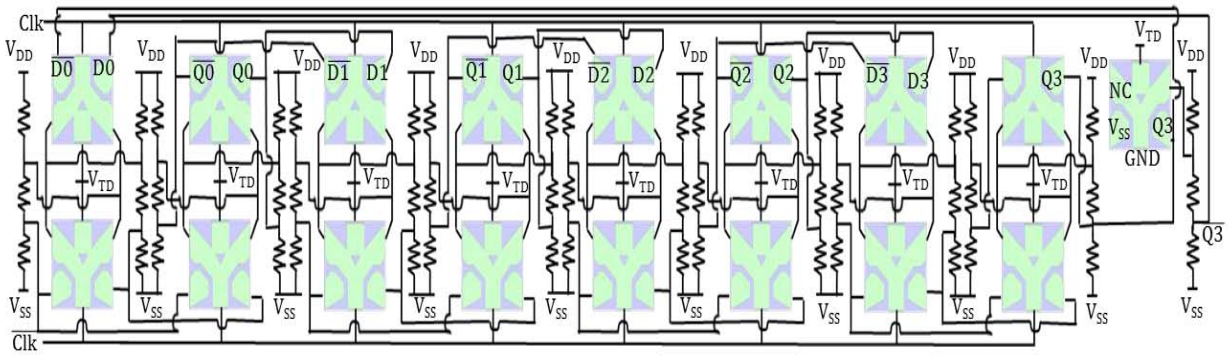


Fig. 14. Implementation of Johnson Ring Counter using BDT based DFFs. The circuit is similar to BDT 4-bit shift register with an extra inverter added. The inverter left drain is not connected (NC) and right gate and left gate are connected to Q3 and V_{SS} respectively.

VII. Sequential Circuits Using BDT DFF

A. Shift Register

Shift Registers are the most common building blocks of ICs. They are widely used in many applications [27], [28] such as digital filters [29], communication receivers [30] and image processing ICs [31]–[33]. In this paper, we implemented a traditional 4-bit serial-input-serial-output (SISO) shift register developed using BDT based DFF mentioned in the previous section of this paper. We have arranged the 4 BDT DFFs in series. The clocks of the DFFs are connected to single clock signal CLK and output of one DFF is connected to input of the next DFF as shown in Fig. 10. At each clock cycle, the data is shifted one bit position to the right. To illustrate the serial shift register, we provided an input data signal DataIn as 1010 as shown in Fig. 11. The output signal of Q3 is connected to DataOut. Table IV indicates the correct logic functionality of the 4-bit SISO shift register.

Since the value of clock signals being independent to value of data signals and vice versa, all the four different kinds of shift registers, serial-input-serial-ouput (SISO), parallel-input-serial-output (PISO), serial-input-parallel-output (SIPO) and parallel-input-parallel-outputs (PIPO) can also be realized using the BDT based DFFs.

B. Frequency Dividers

The present day processing systems work with multiple clock speeds and frequency dividers are the fundamental blocks in generating multiple clock speeds from a single voltage controlled oscillator (VCO) source. Circuits using frequency dividers are used in applications ranging from radar, imaging and point-to-point communications. In this subsection, we implement a frequency divider circuit developed using BDT based DFFs.

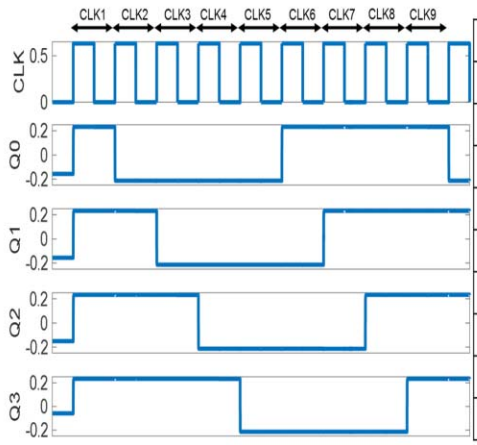
Fig. 12, shows the frequency divider circuit implemented with DFFs based on BDTs. In a conventional CMOS design, a DFF whose complementary output when connected as input to the same DFF, acts as divider-by-2 circuit. However, in case of BDT technology, this cannot be realized. That is because, before the beginning of clock signal, the output signals Q and $\overline{Q}$ both are at logic high levels. In order to eliminate this kind of situation, we are adding an inverter at the end of the DFF. The output of the Q will be connected to right gate of the inverter and the V_{SS} is connected to left gate of the inverter. The left drain terminal is provided with no connection (NC) and the right drain terminal is connected to string of resistors and the output $\overline{Q}$ is connected. This connection ensures that Q and $\overline{Q}$ are always complementary signals to each other.

The clock signals are provided with input frequency f. The output signals Q and $\overline{Q}$ are generated with a clock frequency of $f \div 2$. The development of high frequency divide-by-2 circuit can achieve the highest frequency of 250GHz as output frequency.

The magnitude of clock signals is different from the values of voltage at the output of DFF. Further, in case of realizing a frequency divide-by-4 circuit using the developed divide-by-2 circuit as shown in Fig. 13(a), we have to add more node in the string of resistors and optimize the value of those resistors such that the output voltage values of other nodes Q_1 and $\overline{Q_1}$ will be same as that of Clk and $\overline{Clk}$ respectively. In the proposed DFF, we have utilized a string of resistors as current-to-voltage converter, connected to V_{DD} and V_{SS} as shown in Fig. 13(b). The Q voltage value depends on the current I_D coming from the drain terminal and it cannot be D or Clk signal value simultaneously. One possible solution for this problem is to add more resistors in the string of resistors from V_{DD} to V_{SS} and divide the voltage accordingly such that required output voltages (values of Q and Clk) are obtained as shown in Fig. 13(c). Thus these DFFs can be realized to obtain voltage ranges of Q and Clk simultaneously enhancing the possibility of divide-by-N sequential circuits developed using BDTs.

C. Johnson Ring Counters

Johnson ring counters are another set of sequential circuits that are widely used in VLSI circuits. They are generally used to provide a specific pattern of data sequence by shifting the value in a synchronous manner. The developed BDT based sequential circuit design utilizes the concepts of both BDT based shift registers and BDT based frequency divider. Fig. 14 shows the 4-bit Johnson Ring Counter circuit developed using BDT based DFFs. The DFFs are connected in series to each other, similar to shift register, and an inverter is added to the last DFF Q3 so that Q3 and $\overline{Q}3$ will be complementary to each other. Simulation results of developed Johnson Ring Counter are presented in Fig. 15.



CLK	Q3	Q2	Q1	Q0
1	1	1	1	1
2	1	1	1	0
3	1	1	0	0
4	1	0	0	0
5	0	0	0	0
6	0	0	0	1
7	0	0	1	1
8	0	1	1	1
9	1	1	1	1

Fig. 15. Simulation results of developed Johnson Ring Counter

In this circuit, all the DFFs are getting clock pulses at every state. Data is shifting at every state by the DFF. In total, 8 clock pulses are required to operate a 4-bit Johnson counter in one cycle. The clock pulse starts the cycle at 1st state with sequence 1111 and ends the cycle at 8th state with sequence 0111. The clock pulse at 9th state starts new cycle with sequence 1111.

VIII. Conclusion

Functional simulations are highly useful in developing and analyzing logic circuits using emerging devices at the preliminary stage of the research. In this paper, we developed various traditional sequential circuits such as Shift Registers, Frequency Dividers and Johnson Ring Counters, using a new level-sensitive D-latch that is based on a BDT structure. The D-latch has been developed using a predictive model, based on results of MC simulations that are able to correctly reproduce the complex behavior of BDT for different dielectrics. The simulation results have indicated a successful functionality of developed sequential circuits. Our future work will include but not limit to estimate the power consumption of the developed BDT based D-latch, design a fabricated experiment and characterize the D-latch using THz testing equipment, to design a D-latch using alternate BDT connection methods. We also aim to address the challenges provided by interconnects that dominate delay. We hope that with better interconnects and less parasitics, the developed circuits will play an significant role in future data processing and storage systems.

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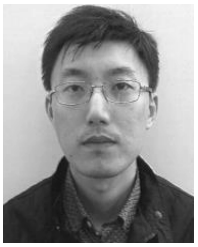

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