Design Optimization of AlInAs–GaInAs HEMTs for Low-Noise Applications

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***Abstract*—In order to optimize the low-noise performance of 50-nm-gate AlInAs–GaInAs high-electron mobility transistors (HEMTs), by using an ensemble Monte Carlo simulation we study the influence of three important technological parameters on their noise level: The doping of the δ-doped layer, the width of the devices and the length of the recess. The noise behavior of the devices is firstly analyzed in terms of the physics-based P, R, and C parameters, and then characterized from a practical (circuit oriented) point of view through their four noise parameters: Minimum noise figure, $F_{\min}$, noise resistance, R_n, and complex input admittance, $Y_{\rm opt}$ (or reflection coefficient, $\Gamma_{\rm opt}$). We have observed an enhancement of the noise when the δ-doping or the device width are increased (a deterioration parallel to that of $f_{\max}$). Thus, the optimum noise operation is obtained for the lowest possible values of the δ-doping and device width. However, for small width the effect of the offset parasitic capacitances makes $F_{\min}$ increase, thus, imposing a limit for the reduction of the noise. Moreover, the increase of R_n for small W makes the noise tuning condition critical to reach the optimum low-noise operation. We have also confirmed that when shortening the recess length from 100 to 20 nm at each side of the gate $F_{\min}$ is reduced, with a slight deterioration of $f_{\max}$, while the static characteristics are not modified.**

***Index Terms*—AlInAs–GaInAs, high-electron mobility transistors (HEMTs), high-speed devices, minimum noise figure, Monte Carlo (MC) simulation, noise parameters, parasitic resistances and capacitances, semiconductor device design and fabrication.**

I. Introduction

ONE OF THE main problems found when trying to increase the operating frequency of a given active device is the degradation of the signal-to-noise ratio; in other words, the signal being amplified is hidden by the fluctuations generated by the device. This problem is enhanced when dealing with low amplitude signals, originating from far emitters (as in the case of satellite communications, radio astronomy or remote sensing applications), or due to power constraints (as in the case of mobile phones). Therefore, the improvement of the frequency performance of the devices must achieve not only the highest possible values of f_t (current gain cuttoff frequency) and $f_{\max}$ (maximum frequency of oscillation), but also the lowest possible levels of noise. Nowadays, 0.1 μm gate InP-based AlInAs–GaInAs–InP pseudomorphic HEMTs (PHEMTs) have reached minimum noise figures as low as 1.4 dB with associated gain of 7.0 dB at 94 GHz [1], and MMICs based on similar devices are able to operate in the 180–205 GHz band [2] with a gain of 20 dB and noise figures of around 10 dB. Moreover, with the use of cryogenic cooling the noise performance of the amplifiers can be greatly improved [3] even at such high frequencies.

In a recent work [4], we performed an analysis of the static and dynamic characteristics of 50- and 100-nm-gate $Al_{0.48}In_{0.52}As$–$Ga_{0.47}In_{0.53}As$ HEMTs, focusing on the influence of the gate length, δ-doping level and width of the devices, W, on their cutoff frequencies. It was carried out by means of a semiclassical two-dimensional Monte Carlo (MC) model whose validity was checked in previous works by obtaining favorable comparisons with experimental results of static characteristics, small signal behavior and noise performance of an InP lattice matched 100-nm-gate HEMT [5]. Using the same tool, in this work we optimize the design of the 50-nm-gate HEMTs in order to improve their noise behavior. The information provided in this paper can be of great interest for device designers when fabricating new devices with different parameters to be optimized (W, recess length, δ-doping) in order to obtain the best low-noise performances. The use of the MC method has an important advantage over other techniques when dealing with the calculation of noise: No assumption is made about the values, correlation or location of the noise sources. On the contrary, the microscopic noise sources (the individual scattering mechanisms) are intrinsically accounted for.

In the next section, we present the parameters that will be used to completely characterize the noise of the HEMTs. Then, in Sections III and IV, we will try to improve the HEMT low-noise performance by optimizing the doping level of the δ-doped layer and the device width, respectively. In Section V we will study other parameter that does not practically affect the static characteristics but can be used to reduce the noise level of the devices; the length of the recess.

II. Noise Parameters

For the noise characterization of the devices it is necessary, first, to calculate the intrinsic noise, characterized by the frequency-dependent spectral densities of the drain- and gate-current fluctuations and its cross-correlation, S_{i_d}, S_{i_g}, and $S_{i_g i_d}$, respectively. However, from the point of view of practical applications, it is much more useful to describe the noise behavior

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of the transistors through their four noise parameters: minimum noise figure, $F_{\min}$, noise resistance, R_n, and the real and imaginary parts of the complex optimum admittance, $Y_{\rm opt}$ (or its equivalent complex reflection coefficient, $\Gamma_{\rm opt}$). From the four noise parameters, in addition to $F_{\min}$, one knows the admittance to be connected at the input of the device to obtain the optimum noise behavior (the associated gain, $G_{\rm ass}$, is just the power gain of this configuration). For the determination of these extrinsic noise parameters, apart from the intrinsic noise calculated with the MC simulation, the parasitic elements of the equivalent circuit (mainly the contact resistances, R_s, R_g, and R_d and capacitances) must be also considered [4]–[8]. For the parasitic elements we have taken typical values obtained experimentally: $L_s = 1$ pH, $L_g = L_d = 25$ pH, $C_{\rm pg} = 1$ fF, $C_{\rm pd} = (220\ {\rm fF/mm}) \times W$, $R_g = (250\ \Omega/{\rm mm}) \times W/3n^2$ (n is the number of gate fingers, which in this work will be always 2), $R_s = (0.25\ \Omega \cdot {\rm mm})/W$ and $R_d = (0.35\ \Omega \cdot {\rm mm})/W$ (see the small signal equivalent circuit presented in [4]). It is important to remark that, since R_s and R_d are inversely proportional to W and R_g is proportional to W, the extrinsic $F_{\min}$ will not be independent of the device width [5]. Another noise parameter which is important from a practical point of view is the noise figure with matched input. It is usually called $F50$ (and the corresponding gain $G50$). Even if from a physical point of view $F50$ and $G50$ do not add any new information to the study of noise in the device, they are very important for circuit design and noise parameter extraction ($F50$ is often employed to experimentally determine the value of R_n [8]).

III. Influence of the δ-Doping

Fig. 1 presents $F_{\min}$, $F50$, $G_{\rm ass}$ and $G50$ at 94 GHz (W-band) under optimum noise bias conditions ($V_{\rm ds} = 0.5$ V) for the 50- and 100-nm-gate HEMTs described in [4]. The simulated layer structure of the 50-(100-nm)–gate HEMTs consists of an $Al_{0.48}In_{0.52}As$ buffer followed by a 10-(25-nm)-thick $Ga_{0.47}In_{0.53}As$ channel, three layers of $Al_{0.48}In_{0.52}As$ [a 2-nm (5-nm) spacer, a δ-doped layer modeled as a 5-nm-thick layer, and a 5-nm (10-nm) Schottky layer] and finally a 10-nm-thick $Ga_{0.47}In_{0.53}As$ cap layer ($N_D = 5 \times 10^{18}$ cm^{-3}). As in the case of $f_{\max}$ [4], a higher δ-doping constitutes a drawback for the noise: $F_{\min}$ of the devices is deteriorated. In the inset it is observed that R_n increases with the δ-doping, indicating that, in addition to the deterioration of $F_{\min}$, the noise factor is more sensitive with respect to changes in the input impedance. Consequently, the difference between $F50$ and $F_{\min}$ is more significant for higher δ-dopings. Fig. 1(b) also shows that $G50$ is lower than $G_{\rm ass}$; when the noise tuning condition at the input is not maintained, in addition to the increase of the noise figure, a decrease of the gain in the circuit takes place. Anyway, for the same δ-doping of 5×10^{12} cm^{-2}, the 50-nm HEMT has a lower $F_{\min}$ than the 100-nm device, 2.4 against 3.0 dB for currents around 50 mA/mm, with much higher f_t and $f_{\max}$ [4]. Another advantage of reducing the gate length, from the point of view of low-noise operation, is the increase of $G_{\rm ass}$ [Fig. 1(b)].

The behavior of $F_{\min}$, mainly at high frequency, cannot be explained by means of simple approximations like those used in classical models for long-channel devices, since some important elements of the small signal equivalent circuit of the devices

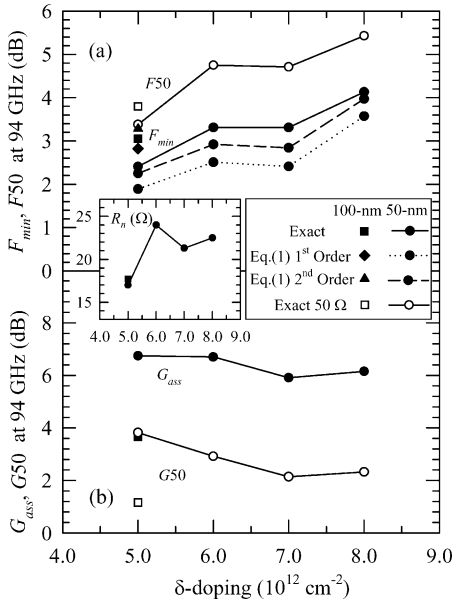

Fig. 1. (a) $F_{\min}$ and $F50$ and (b) $G_{\rm ass}$ and $G50$ (and R_n in the inset) at 94 GHz for the $V_{\rm gs}$ corresponding to optimum noise bias conditions ($V_{\rm ds} = 0.5$ V) in the 100-nm and 50-nm HEMTs with $W = 100$ μm as a function of the δ-doping. The values obtained for $F_{\min}$ by using the exact calculation are compared with those estimated through (1) truncating the series at the first and second order on (f/f_c).

($C_{\rm ds}$, $C_{\rm gd}$ and g_d) are not considered [9], [10]. Following Pucel *et al.* [10] $F_{\min}$ can be calculated as a power series of the frequency, f, through

$$F_{\min} = 1 + 2\frac{f}{f_c}\frac{T}{T_o}\sqrt{K_g\left[K_r + g_m(R_s + R_g)\right]} + 2\left(\frac{f}{f_c}\right)^2 \frac{T}{T_o} K_g g_m \left(R_s + R_g + K_c R_i\right) + \cdots \quad (1)$$

with

$$K_g = P + R - 2C\sqrt{\rm PR} \quad (2)$$

$$K_c = \frac{P - C\sqrt{\rm PR}}{P + R - 2C\sqrt{\rm PR}} \quad (3)$$

$$K_r = \frac{\rm PR\left(1 - C^2\right)}{P + R - 2C\sqrt{\rm PR}} \quad (4)$$

where $P = S_{i_d}/4K_BT|Y_{21}|$ and $R = S_{i_g}|Y_{21}|/4K_BT|Y_{11}|^2$ are the well–known normalized drain and gate noise coefficients and $C = {\rm Im}\lfloor S_{i_g i_d}\rfloor/\sqrt{S_{i_g} S_{i_d}}$ the correlation factor (where Y_{11}, Y_{12}, Y_{21}, and Y_{22} are the intrinsic Y parameters of the HEMT). T and T_o are the ambient and the reference temperature, respectively. R_i is the source-to-channel resistance and $f_c = g_m/2\pi(C_{\rm gs} + C_{\rm gd})$ the intrinsic cutoff frequency. For low frequencies ($f \ll f_c$) (1) can be simplified by truncating the series at the second order term, or even just at first order [9]. The values of $F_{\min}$ at 94 GHz calculated through (1), both at first and second order approximations, are shown in Fig. 1 together with the exact values obtained from the MC simulations with the method described in [5]. As observed, the model works well only if the term on $(f/f_c)^2$ is taken into account, since under minimum noise biasing conditions the value of f_c is not much higher than 94 GHz. It is also important to remark that to reach this good agreement it is necessary to use the exact frequency

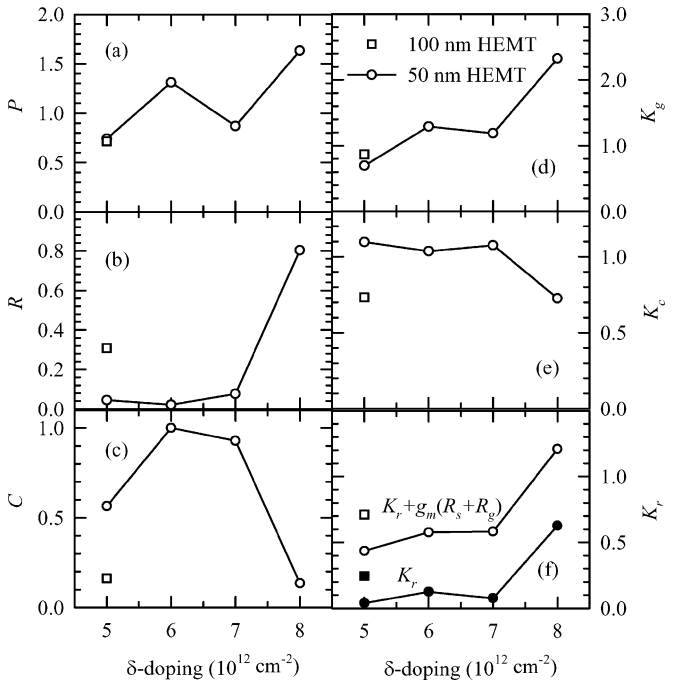

Fig. 2. (a) P, (b) R, (c) C, (d) K_g, (e) K_c, and (f) K_r at 94 GHz for the bias point of optimum noise ($V_{\rm ds} = 0.5$ V) in the 100-nm (squares) and 50-nm (circles) HEMTs with $W = 100$ μm as a function of the δ-doping. In (f), the value of $g_m(R_s + R_g)$ is also shown.

dependent P, R, C, and Y parameters, obtained from the MC calculation of the noise spectral densities, and the dynamic response of the devices [5].

In Fig. 2 the values of P, R, C, K_g, K_r and K_c under minimum noise biasing conditions are shown as a function of the δ-doping. The increase of both P and R when raising the δ-doping [Fig. 2(a) and (b)], is related to the parasitic conduction through the δ-doped layer. The appearance of a parasitic channel enhances, first, the drain current fluctuations, and thus, the value of P, due to the velocity fluctuations related to the considerable number of real-space-transfer mechanisms [11] (electrons going out from the InGaAs channel). Second, the capacitive coupling between the gate and the charge fluctuations in the channel is strengthened, and thus, the gate current fluctuations increase. This effect is similar to that of a higher $V_{\rm gs}$, which leads to the increase of R in short-channel HEMTs, a trend that has already been experimentally measured [12] and numerically confirmed [13]. Fig. 2(c) shows that the value of C approaches 1.0 for intermediate δ-dopings, in agreement with the widespread Pospieszalsky's model [14]. However, C strongly decreases for $\delta = 8 \times 10^{12}$ cm^{-2}, due to the decoupling of the gate and drain current fluctuations induced, again, by the more frequent real space transfer mechanisms. Thus, the dependence of P, R and C (and also that of K_g, K_r and K_c) on the δ-doping agrees well with previous analyzes of these parameters in short-channel HEMTs [9], [10]. In Fig. 2(f) it can be observed that (mainly for low δ-dopings) most of the noise of the device is originated by the parasitic resistances, since the term $g_m(R_s + R_g)$ predominates over the value of K_r, which represents in first order approximation the intrinsic contribution to the noise. Examining (1), one may consider that increasing f_c the noise behavior of the devices should be improved, however, $F_{\rm min}$ increases. From the results in Fig. 2 it can be concluded that the increase of $F_{\rm min}$ with the δ-doping comes from: 1) the higher values of K_g and K_r, related to the increase of the intrinsic drain and gate noise, represented respectively through P and R, and 2) the larger extrinsic noise, originated by the increase of g_m, that leads to a stronger amplification of the fluctuations generated at the source and gate resistances.

IV. Influence of the Device Width

The dependence of $F_{\rm min}$ on the device width was widely discussed in [5], where we demonstrated that for the 100-nm-gate HEMT $F_{\rm min}$ is lowered when reducing W due to the important effect of R_g on the noise level. The same trend can be observed in the 50-nm-gate devices, whose $F_{\rm min}$ is deteriorated for longer W due to the increase of R_g. However, the model used in [5] for the extrinsic capacitances does not take into account the offset capacitances, which, as shown in [4], are very important for the dynamic response of the HEMTs. These offset capacitances represent the part of the extrinsic gate-source and gate-drain capacitances which is not dependent on the device width (calculated by extrapolating their values to $W = 0$), and their origin is the fringing geometric capacitance between contacts pads. In order to show the effect of these capacitances on the noise behavior, the values of $F_{\rm min}$ and $G_{\rm ass}$, together with those of $F50$ and $G50$, are plotted in Fig. 3 as a function of W for three different offset values (no offset, 1 fF and 3 fF). It can be observed how the reduction of the offset parasitic capacitances is very important for the improvement of the low-noise operation of the HEMTs (decrease of $F_{\rm min}$ and increase of $G_{\rm ass}$), mainly when W is lower than 50 μm. Therefore, the value of W for an optimum noise performance must be chosen as a tradeoff between the small width needed to minimize the gate resistance and the sufficiently large one necessary to decrease the effect of the offset parasitic capacitances. This is a very important point, since W must be reduced when increasing the operation frequency of the devices in order to avoid problems of matching, and, as a consequence, the degradation due to the offset capacitances can become significant. Again, for the optimization of the low-noise operation of the HEMTs (as it happened with the dynamic behavior), special care must be taken in their design to diminish the value of the offset parasitic capacitances. For example, as stated in [12], the use of single finger gates, for which the offset capacitances are lower than with typical multifinger gates, can be very useful for improving the low-noise operation of HEMTs at high frequency. Indeed, at very high frequencies the offset capacitances become the limiting parameter for the reduction of $F_{\rm min}$ instead of the gate resistance, which typically is very low for the small values of W adopted for high-frequency operation.

The values we have obtained for $F_{\rm min}$ and $G_{\rm ass}$ are not as good as those measured in the state-of-the-art 0.1 μm-gate PHEMT presented in [1] ($F_{\rm min} = 1.4$ dB, $G_{\rm ass} = 7.0$ dB). This is due to the excellent gate contact technology used in [1], able to considerably reduce the value of R_g, thus minimizing the extrinsic contribution to $F_{\rm min}$, which in our case is the major source of noise (mainly for large W), Fig. 2(f).

In Fig. 3 it can be also observed that the effect the offset parasitic capacitances have in $F50$ is quite small. This is so because when reducing W, though the offset parasitic capacitances originate the degradation of $F_{\rm min}$, this is compensated by a reduction of

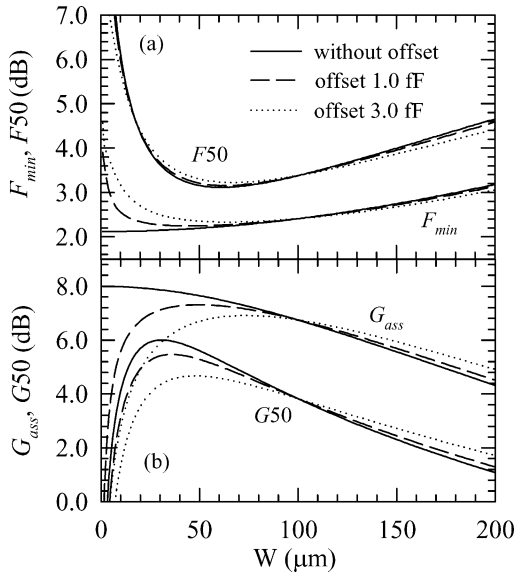

Fig. 3. (a) $F50$ and $F_{\min}$ and (b) $G50$ and $G_{\rm ass}$ at 94 GHz in the 50-nm HEMT with $\delta = 5 \times 10^{12}$ cm^{-2} as a function of the width of the devices. Three different models for the extrinsic capacitances are used: without offset (solid lines), with offset of 1 fF (dashed lines), and 3 fF (dotted lines).

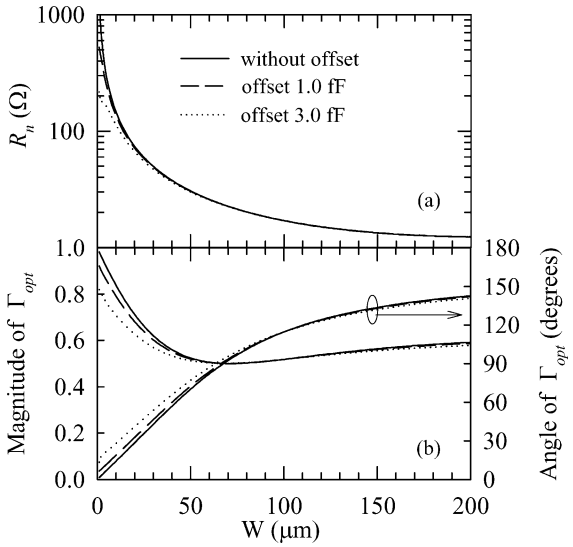

Fig. 4. (a) R_n and (b) magnitude and angle of $\Gamma_{\rm opt}$ at 94 GHz in the 50-nm HEMT with $\delta = 5 \times 10^{12}$ cm^{-2} as a function of the width of the devices without offset capacitances (solid lines), with offset of 1 fF (dashed lines) and with offset of 3 fF (dotted lines).

R_n and $|\Gamma_{\rm opt}|$. Indeed, as observed in Fig. 4(a) and (b), the values of R_n and $|\Gamma_{\rm opt}|$ increase sharply for small W, but are lower the higher the offset capacitances. In the case of $G50$, the degradation caused by the offset capacitances is stronger, since they enlarge the input power mismatch for a 50-Ω input impedance.

We can conclude that for high-frequency applications, when W must be small: 1) the noise tuning condition becomes critical for the optimum low-noise performance of the devices, since small deviations of the input admittance from $Y_{\rm opt}$ lead to a rapid increase of the noise figure, mainly due to the high value of R_n; and 2) the design efforts in order to reduce the value of the offset capacitances are practically worthless if the noise tuning condition is not perfectly fulfilled.

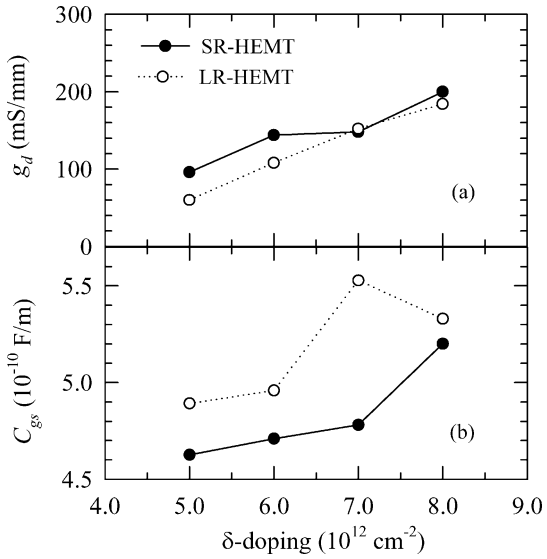

Fig. 5. (a) g_d and (b) $C_{\rm gs}$ for the bias point of optimum noise ($V_{\rm ds} = 0.5$ V) in the 50-nm gate HEMTs as a function of the δ-doping. Two different recess lengths have been used in the simulations, a long one of 100 nm for the LR-HEMTs (dotted lines, open circles) and a short one of 20 nm for the SR-HEMTs (solid lines, black circles).

V. Influence of the Recess Length

In addition to the δ-doping and W, another parameter that can modify the noise characteristics is the geometry of the recess. The recess length has a significant influence on the potential profile inside the devices. If it is enlarged, the high electric fields appearing between gate and drain can be somewhat reduced, attenuating hot carriers effects and impact ionization mechanisms, and thus moving to higher $V_{\rm ds}$ the degradation of the device characteristics (and mainly the noise) related to the appearance of kink effect.

In order to study the influence of the recess length on the frequency and noise performance of the devices we have simulated 50-nm HEMTs with a shorter recess length, 20 nm at each side of the gate (denoted by SR-HEMTs) instead of the 100 nm of the previously simulated HEMTs (denoted by LR-HEMTs). These values of the recess lengths are, respectively, the minimum and the maximum values allowed by the wet etching technique (with a mixture of succinic acid, ammonia, and hydrogen peroxide) used to selectively remove the GaInAs cap layer and define the recess. More details about the technological process can be found in [15]. The static characteristics of the SR-HEMTs are practically the same as those shown in [4] for the LR-HEMTs, since the width of the channel does not depend on the recess length. However, some differences appear when dealing with the dynamic behavior: g_d increases [Fig. 5(a)] and $C_{\rm gs}$ decreases [Fig. 5(b)] when reducing the recess length, in qualitative agreement with the usual results found in real devices. This behavior can be explained as a consequence of 1) the stronger injection of electrons into the buffer, related to the higher electric fields (higher g_d), and 2) the complete depletion of the δ-doped plane in the near-gate region induced by the surface charges located at the recess, which reduces the lateral contribution to the gate capacitance (lower $C_{\rm gs}$).

Before studying the noise parameters we will compare the dynamic behavior of the LR- and SR-HEMTs. For a better com-

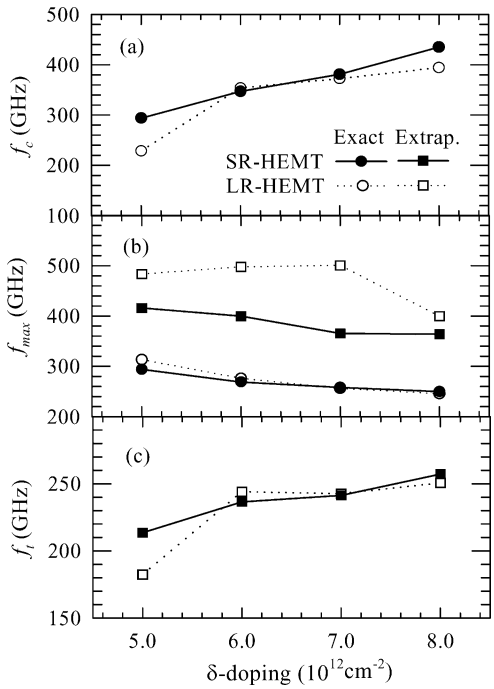

Fig. 6. Maximum values of (a) f_c, (b) $f_{\max}$ (exact and extrapolated) and (c) f_t in the 50-nm gate LR- and SR-HEMTs with $W = 100\,\mu$m ($V_{\rm ds} = 0.5$ V) as a function of the δ-doping.

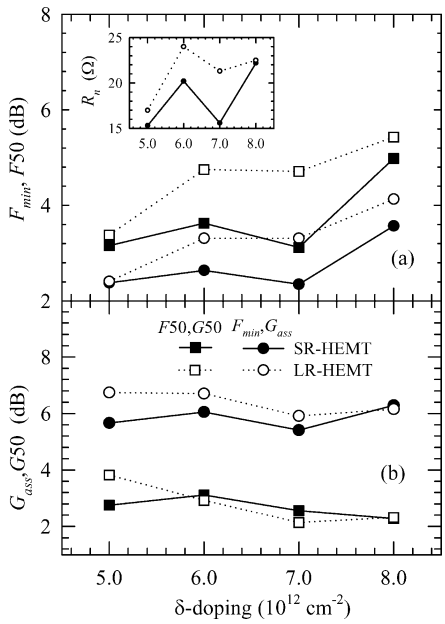

Fig. 7. (a) $F_{\min}$ and $F50$ (the inset shows R_n) and (b) corresponding $G_{\rm ass}$ and $G50$ at 94 GHz for the optimum noise bias point ($V_{\rm ds} = 0.5$ V) in the SR- and LR-HEMTs as a function of the δ-doping.

parison of the intrinsic and extrinsic frequency performance of the different devices, the maximum values of f_c, $f_{\max}$ and f_t are plotted in Fig. 6 as a function of the δ-doping. For $f_{\max}$ both exact and extrapolated values are shown [4]. As observed, the decrease of $C_{\rm gs}$ leads to a higher f_c in the SR-HEMT with respect to the LR-HEMT [Fig. 6(a)]. However, we have to note that the intrinsic cutoff frequency of the devices, f_c, does not take into account the variation of g_d. Conversely, the value of g_d is quite important for the extrinsic behavior of the HEMTs. Thus, its increase degrades the value of $f_{\max}$ when reducing the recess length [Fig. 6(b)]. The degradation of $f_{\max}$ is larger in the extrapolated values than in the exact ones. This happens because the increase of g_d reduces the unilateral gain U, but a supplementary effect due to a lowered positive feedback associated to the term $(g_m/g_d)C_{dc}$ takes place, and this second effect affects only the calculation of the extrapolated $f_{\max}$. The values of f_t shown in Fig. 6(c) only exhibit some differences between LR- and SR-HEMTs for $\delta = 5 \times 10^{12}$ cm^{-2}, while for the higher δ-dopings the results are similar, showing a behavior analogous to that of f_c.

Finally, concerning the noise performance of the 50-nm-gate LR- and SR-HEMTs, the values of $F_{\min}$ and $F50$ for the optimum noise biasing are represented in Fig. 7 together with $G_{\rm ass}$ and $G50$ as a function of the δ-doping. Both $F_{\min}$ and $F50$ are improved by reducing the recess length due to the lower value of R_n shown in the inset of Fig. 7. Therefore, even if the SR-HEMT have a slightly worse performance than the LR-HEMT in terms of $f_{\max}$, it exhibits a better low-noise operation due to the reduction of $C_{\rm gs}$ [Fig. 5(b)]. We have confirmed that the decrease of $F_{\min}$ achieved by means of a short recess is just associated to the higher cutoff frequency, since the values of the P, R and C parameters (and consequently those of K_g, K_r and K_c) remain practically unchanged. With regard to the gains [Fig. 7(b)], the values of $G_{\rm ass}$ and $G50$ are comparable in the SR- and LR-HEMTs, around 6 and 3 dB, respectively.

The recess length has some influence on the electric field profile inside the devices. A slight reduction is observed in the maximum value reached by the electric field in the LR-HEMT as compared to the SR-HEMT. However, for intrinsic $V_{\rm ds}$ values up to 0.5 V, as those analyzed here, it does not imply a noticeable benefit in terms of impact ionization. The differences related to impact ionization come into sight when further increasing $V_{\rm ds}$. Indeed, the appearance of the kink effect is strongly dependent on the geometry of the recess. In these conditions noise is abruptly increased and the prevention of impact ionization by increasing the recess length can be very useful. However, the study of kink-effect-related noise lies beyond the objectives of this paper and will be the subject of future works.

VI. Conclusion

By using a two-dimensional MC model, an optimization of the low-noise behavior of 50-nm HEMTs has been performed by determining the optimum values of δ-doping, device width and recess length. Analogously to what we found in [4] when dealing with the dynamic behavior of the HEMTs, the noise level is deteriorated with the increase of the δ-doping. Therefore, its value must be as low as possible while maintaining a sufficient level of current. A decrease of $F_{\min}$ is observed when reducing W, with a lower limit imposed by the offset value of the parasitic capacitances, that degrade the low-noise operation for small W. Moreover, the increase of R_n for low W leads to a considerable increase of $F50$, thus being critical to work at the optimum matching conditions in order to achieve a low noise level. This is especially delicate in devices fabricated for high frequency operation, where W must be very small to make possible the input matching. We have also confirmed that when reducing the recess length the I-V characteristics of HEMTs are

almost unchanged, but a slight degradation of $f_{\max}$ (due to the increase of g_d) and an improvement of $F_{\min}$ and $F50$ (due to the reduction of $C_{\rm gs}$) with similar gains are obtained.

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