Monte Carlo Determination of the Intrinsic Small-Signal Equivalent Circuit of MESFET's

Tomás González and Daniel Pardo

Abstract—**A Monte Carlo technique for the determination of the intrinsic elements of a broad-band small-signal equivalent circuit (SSEC) of MESFET's (and FET's in general) is described. The values of the different elements are calculated from the Y parameters of the intrinsic MESFET, which are obtained from the Fourier analysis of the device transient response to voltage-step perturbations at the drain and gate electrodes. An accurate estimator of the instantaneous currents at the terminals is used, which guarantees the precision of the method. Three different MESFET geometries have been analyzed. For low drain currents under saturation the intrinsic elements are found to be independent of frequency in the whole range of device operation. This fact validates the technique and the proposed equivalent circuit under these conditions. However, for high drain currents the gate-drain capacitance and the drain conductance depend on frequency due to the appearance of charge-accumulation effects.**

I. Introduction

In the design of microwave circuits, the knowledge of an accurate small-signal equivalent circuit (SSEC) of a FET is a helpful tool to characterize the device behavior. For example, it is useful for the analysis of the FET noise performance [1], [2] and for the determination of the gain, cut-off frequency, etc. [3]. The frequency range in which the equivalent circuit can be applied is specially important. So, broad-band models are to be developed.

Usually, the SSEC of a FET is designed by choosing a topology so that each element provides a lumped approximation to some physical aspect of the device [4], [5]. Although there is no fixed standard equivalent circuit to describe a transistor, a SSEC which is commonly accepted is formed of fifteen different frequency-independent elements: eight of them corresponding to the external parasitic effects and normally considered independent of the bias point, and the other seven describing the intrinsic behavior of the FET and dependent on the biasing conditions.

The experimental characterization of the FET behavior at high frequencies involves the measurement of the S parameters. The fifteen elements of the equivalent circuit must be obtained from them. An extraction technique was proposed by Minasian [6], extended by Dambrine *et al.* up to 5 GHz [7], and finally developed for the whole frequency range of FET operation by Berroth and Bosch [8]. The main difficulty implied in this technique is the evaluation of the external elements, in order to get the Y parameters of the intrinsic device. This is done by "cold modeling" of the equivalent circuit [7], [9] and by performing several transformations of the measured S parameters, so that finally the intrinsic Y parameters are de-embedded from them.

By using this extraction technique, and avoiding the evaluation of the external elements, in this paper we describe a theoretical procedure to calculate the intrinsic elements of the FET SSEC starting from the Y parameters obtained by means of a Monte Carlo (MC) particle simulation. The MC method includes all the processes relevant to the transport in small semiconductor devices (non-stationary effects, hot carriers, etc.). Moreover, it is very well suited to analyze the intrinsic behavior of a device, like shown in [10] for the case of noise, closely related to the small-signal behavior. With the MC simulation one can be sure that no parasitic effect is involved, so that the validity of the intrinsic SSEC proposed can be verified by checking the frequency dependence of the calculated elements. For a given operating point, the Y parameters are obtained from the Fourier analysis of the device transient response to voltage-step perturbations at the drain and gate terminals. The success of this analysis depends crucially on the accuracy of the values calculated for the instantaneous currents at the terminals during the transient. In our case, the transient currents are accurately evaluated by using the efficient technique proposed in [11].

As application we have determined the SSEC for the case of GaAs MESFET's. Three different geometries and their influence on the elements of the equivalent circuit have been analyzed. The MC particle simulation provides the physical background of the differences found among them in terms of particle dynamics and self-consistent fields.

The paper is organized as follows. In Section II, the theoretical basis and the different steps of the technique are presented. In Section III, the details of the physical model, concerning the MC particle simulation and the MESFET geometries considered, are described. The results of the simulations are given and discussed in Section IV. Finally, the main conclusions are drawn in Section V.

II. Theoretical Analysis

There are several methods to calculate the Y parameters [12]. Here we employ the Fourier decomposition of the FET response to transient excitations. Let us suppose that over the stationary operating point we apply a voltage-step perturbation of amplitude ΔV_j at terminal j, and that $I_i(t)$ is the response

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The authors are with the Departamento de Física Aplicada, Universidad de Salamanca, Plaza de la Merced s/n, 37008 Salamanca, Spain.

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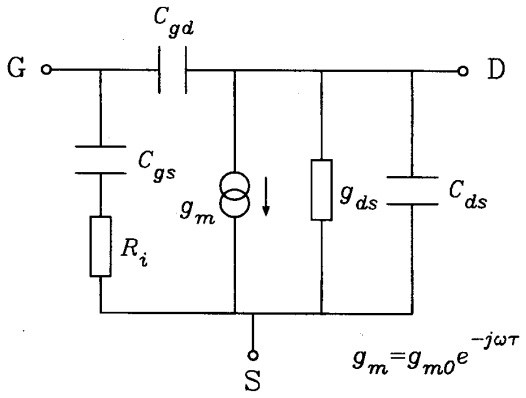

Fig. 1. Small-signal equivalent circuit of the intrinsic FET.

in the current at terminal i. The complex Y_{ij} parameter will be given by the relation between the Fourier components of both signals, and can be shown to be [12]:

$$\mathrm{Re}\,[Y_{ij}(\omega)] = \frac{I_i(\infty) - I_i(0)}{\Delta V_j} + \frac{\omega}{\Delta V_j}\int_0^\infty [I_i(t) - I_i(\infty)] \cdot \sin\omega t\, dt \quad (1)$$

$$\mathrm{Im}\,[Y_{ij}(\omega)] = \frac{\omega}{\Delta V_j}\int_0^\infty [I_i(t) - I_i(\infty)]\cos\omega t\, dt \quad (2)$$

where $I_i(0)$ and $I_i(\infty)$ are the stationary currents at terminal i before and after the voltage perturbation, respectively. The FET transient response is finite in time, so that the integrals in (1) and (2) can be evaluated with a reasonable simulation time, after which it is assumed that $I_i(t) = I_i(\infty)$. In the following, $i = 1$ will stand for the gate and $i = 2$ for the drain.

In order to determine the four Y parameters, two excitations are needed: one in the gate voltage and other in the drain voltage. It must be stressed that the voltage-step amplitude must be sufficiently small so as to avoid harmonic excitation in the device response, and large enough to get significant variations in the currents that dominate over numerical and physical noise. We have applied $\Delta V_1 = 0.125$ V for the case of the gate and $\Delta V_2 = 0.5$ V for the case of the drain.

Although the four Y parameters describe completely the FET small-signal response, the designer is interested in an equivalent circuit with lumped elements associated physically with particular parts of the device. Once the external parasitic elements have been eliminated, the SSEC of the FET reduces to the topology shown in Fig. 1. It is formed of seven intrinsic elements, each of them representing some aspect of the device physics. Thus, C_{ds}, C_{gs} and C_{gd} correspond to the drain-source, gate-source and gate-drain capacitances, respectively. R_i is the resistance of the ohmic channel between the source and the gate. g_{m0} represents the steady-state transconductance, and τ the delay time of the transistor, i.e., the time it takes a signal applied at the gate to reach the drain. g_{ds} is the drain conductance, and its inverse corresponds to the resistance of the conducting channel between the source and the drain.

The elements of this intrinsic equivalent circuit for a given bias point can be obtained from the frequency-dependent Y parameters of the intrinsic FET corresponding to that point. By simple circuit analysis, the following relations between them can be derived [6]:

$$Y_{11}(\omega) = \frac{R_i C_{gs}^2 \omega^2}{D} + j\omega\left(\frac{C_{gs}}{D} + C_{gd}\right) \quad (3)$$

$$Y_{12}(\omega) = -j\omega C_{gd} \quad (4)$$

$$Y_{21}(\omega) = \frac{g_{m0}e^{-j\omega\tau}}{1 + j\omega R_i C_{gs}} - j\omega C_{gd} \quad (5)$$

$$Y_{22}(\omega) = g_{ds} + j\omega(C_{ds} + C_{gd}) \quad (6)$$

with $D = 1 + \omega^2 C_{gs}^2 R_i^2$.

From these expressions, and separating the Y parameters into their real and imaginary parts, the equivalent-circuit elements can be found analytically [8]:

$$C_{gd} = -\frac{\mathrm{Im}\,(Y_{12})}{\omega} \quad (7)$$

$$C_{gs} = \frac{\mathrm{Im}\,(Y_{11}) - \omega C_{gd}}{\omega}\left(1 + \frac{(\mathrm{Re}(Y_{11}))^2}{(\mathrm{Im}\,(Y_{11}) - \omega C_{gd})^2}\right) \quad (8)$$

$$R_i = \frac{\mathrm{Re}\,(Y_{11})}{(\mathrm{Im}\,(Y_{11}) - \omega C_{gd})^2 + (\mathrm{Re}\,(Y_{11}))^2} \quad (9)$$

$$g_{m0} = \sqrt{((\mathrm{Re}\,(Y_{21}))^2 + (\mathrm{Im}\,(Y_{21}) + \omega C_{gd})^2)(1 + \omega^2 C_{gs}^2 R_i^2)} \quad (10)$$

$$\tau = \frac{1}{\omega}\arcsin \cdot \left(\frac{-\omega C_{gd} - \mathrm{Im}\,(Y_{21}) - \omega C_{gs} R_i\,\mathrm{Re}\,(Y_{21})}{g_m}\right) \quad (11)$$

$$C_{ds} = \frac{\mathrm{Im}\,(Y_{22}) - \omega C_{gd}}{\omega} \quad (12)$$

$$g_{ds} = \mathrm{Re}\,(Y_{22}) \quad (13)$$

The way to validate the proposed equivalent circuit is to check the dependence on frequency of the different elements.

III. Physical Model

A. Simulated MESFET's

The present technique has been applied to three different geometries of a GaAs MESFET (which are shown in Fig. 2) in order to analyze their influence on the elements of the SSEC. The device consists of an n^+nn^+ structure with a one-micron channel modulated by a gate contact of 0.5 μm. The source and drain contacts are 0.2 μm long, and are placed at the end of the n^+ regions. In the case of MESFET A, no substrate is considered. The presence of a GaAs semi-insulating substrate is introduced in MESFET B. Finally, the gate is displaced 0.1 μm towards the source in MESFET C.

B. Monte Carlo Simulation

The simulation of the GaAs MESFET's has been performed by coupling self-consistently a two-dimensional Poisson's solver with an ensemble MC simulation, three dimensional in momentum space and two dimensional in real space. The MC procedure follows the standard scheme [3], [13]. The value adopted for the non-considered dimension of the devices

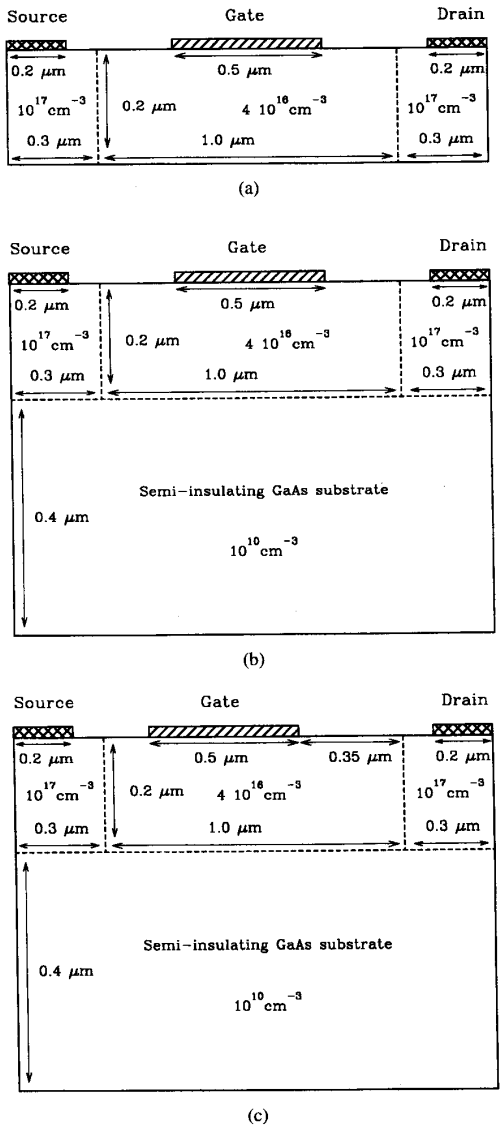

Fig. 2. Cross section of the three MESFET geometries considered: (a) without substrate, (b) with substrate, and (c) with the gate displaced towards the source.

is 0.714 μm, which means an average number of simulated carriers between 9500 and 13000 depending on the bias. The model for the GaAs conduction band is formed of three non-parabolic spherical valleys (Γ, L and X). The scattering mechanisms considered are: intervalley (equivalent and non-equivalent), acoustic, piezoelectric, polar optical, non-polar optical and interaction with ionized impurities. The GaAs physical parameters used in the simulation are the same as those used for the valleys of the first conduction band in previous works [14]. To solve Poisson's equation, a grid formed of 160 × 25 meshes of 100 × 80 Å is used for MESFET A, and a non-uniform grid of 160 × 44 meshes for MESFET's B and C. The electric field is updated each time step of 10 fs. Dirichlet (fixed value) and Neumann (zero normal derivative) boundary conditions for the potential are applied respectively at the contacts and elsewhere on the device surface. The source and drain electrodes are treated as ohmic contacts by absorbing all the electrons that hit them and by injecting at each time step a number of carriers which maintains neutrality in the adjacent cells. The Schottky contact at the gate is treated as a perfect absorbing boundary: there is absorption of particles, but no injection. Elsewhere on the device surface the carriers are reflected. The simulation is performed at 300 K.

A critical requirement for the success and exactness of the present technique is to obtain accurate values of the instantaneous currents at the terminals during the transients, including the displacement contribution. To this purpose, the usual approach that is employed consists, for the conduction current, in counting the net number of particles crossing the terminals at each time step and, for the displacement current, in making the time derivative of the electric field at the contacts. This approach, which is appropriate to obtain the average stationary currents, is not sufficiently accurate for the present analysis [15]. Nevertheless, the recent technique proposed in [11] makes possible an improvement in the accuracy of the calculations to the extent of analyzing the intrinsic ac response of the device. With this technique, and for the geometries of the MESFET's in Fig. 2, the currents per unit length at the source, drain and gate at a time $t, I_s(t), I_d(t)$ and $I_g(t)$, are given by:

$$I_s(t) = \frac{1}{x_{g1} - x_s}\left[Q \sum_i^{x_s - x_{g1}} v_{xi}(t) + \frac{\varepsilon_0 \varepsilon_r}{\Delta t} \sum_{j=1}^{M_y} \Delta y_j (\varphi(x_s, y_j, t) - \varphi(x_s, y_j, t - \Delta t) - \varphi(x_{g1}, y_j, t) + \varphi(x_{g1}, y_j, t - \Delta t))\right] \quad (14)$$

$$I_d(t) = \frac{1}{x_d - x_{g2}}\left[Q \sum_i^{x_{g2} - x_d} v_{xi}(t) + \frac{\varepsilon_0 \varepsilon_r}{\Delta t} \sum_{j=1}^{M_y} \Delta y_j (\varphi(x_{g2}, y_j, t) - \varphi(x_{g2}, y_j, t - \Delta t) - \varphi(x_d, y_j, t) + \varphi(x_d, y_j, t - \Delta t))\right] \quad (15)$$

$$I_g(t) = I_s(t) - I_d(t) \quad (16)$$

where $\varepsilon_0 \varepsilon_r$ is dielectric constant of the material, Δt the time step, Q the linear charge density of a particle, v_{xi} the velocity in the x direction of the ith particle, M_y the number of vertical meshes, Δy_j the vertical dimension of the jth vertical mesh, y_j its y position, φ the potential, and x_{g1}, x_{g2}, x_s and x_d the x positions of the left edge of the gate, the right edge of the gate, the right edge of the source and the left edge of the drain, respectively. The summation over i is performed over the particles with x position between x_s and x_{g1} in the case of the source current, and between x_{g2} and x_d in the case of the drain current. Although the carriers outside these regions

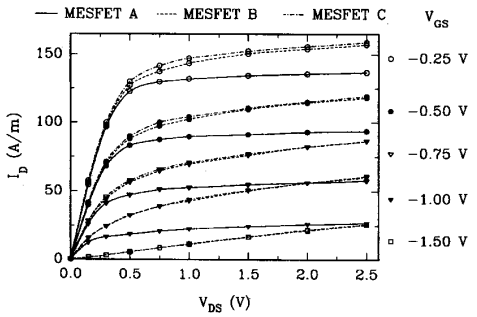

Fig. 3. Drain-current versus drain-voltage characteristics of the three MESFET's analyzed. The gate voltages include the built-in potential of the Schottky contact (−0.7 V).

do not contribute explicitly to the instantaneous currents in (14) and (15), their influence is included through the terms associated to the integration of the time derivatives of the potential at the vertical cross-sections x_s and x_{g1} for $I_s(t)$, and x_{g2} and x_d for $I_d(t)$.

With the aim of reducing the physical noise present in the currents due to the thermal fluctuations in the distribution of fields and particles, a set of ten different simulations has been performed for each of the transients. The values of the currents employed in the calculations of (1) and (2) are evaluated as the average of those obtained in each set of ten simulations.

IV. Results and Discussion

The dc current-voltage characteristics of the three MESFET's considered are shown in Fig. 3. The gate voltage includes the built-in potential of the Schottky contact (−0.7 V). After a short linear dependence, a saturation region appears, which is due to the transfer of carriers to the upper valleys between the gate and the drain, and to the screening effect of the gate on the source region. The saturation is less pronounced in MESFET's B and C due to the flux of current through the substrate. In the case of MESFET C, the current is slightly higher with respect to MESFET B, above all for the lowest values of V_{GS}. Under saturation conditions, the current-gain cut-off frequency, f_T, is about 45 GHz in the three devices.

An example of the transient response currents at the gate and drain terminals to the two voltage-step perturbations needed to get the Y parameters is shown in Fig. 4. The transients correspond to MESFET B at the bias point $V_{GS} = -1.0$ V, $V_{DS} = 1.5$ V. At $t = 0^+$, a spike (whose amplitude exceeds the range shown in Fig. 4) appears in the terminal currents due to the feedback capacitance present in the intrinsic device. This spike is proportional to the time derivative of the applied voltage perturbation and is pure displacement current. To get a proper estimation of the intrinsic capacitances, the correct evaluation of these current spikes is essential [12]. In our case this is assured by the value adopted for the time step in the simulation, 10 fs, which is small enough to this purpose. Although the currents shown in Fig. 4 are the result of averaging ten different transients, noticeable fluctuations due to thermal noise are still detected. The gate current is initially null and, when the voltage perturbation is applied, undergoes

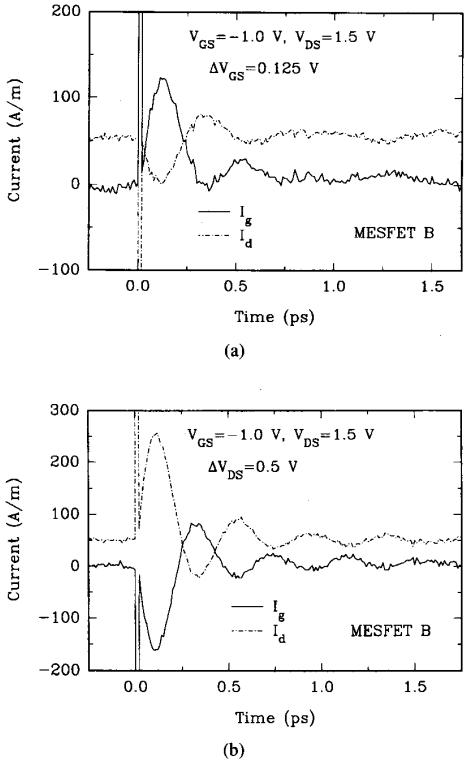

Fig. 4. Transient response in the gate and drain currents of MESFET B to a voltage step of amplitude (a) $\Delta V_{GS} = 0.125$ V, and (b) $\Delta V_{DS} = 0.5$ V applied at $t = 0$ over the stationary point corresponding to $V_{GS} = -1.0$ V, $V_{DS} = 1.5$ V.

a transient due to the displacement current induced by the redistribution of carriers in the channel, after which returns to zero. In the case of the drain current, both displacement and conduction components contribute during the transient, and the initial and final values are different. The duration of the transient changes depending on the operating point.

The intrinsic Y parameters obtained from the transients of Fig. 4 by means of (1) and (2) are shown in Fig. 5. It can be observed that their frequency dependence coincides with that predicted by (3)–(6). Thus, $\mathrm{Re}\,(Y_{22})$ is practically constant with frequency, $\mathrm{Re}\,(Y_{12})$ is null, $\mathrm{Im}\,(Y_{22})$ and $\mathrm{Im}\,(Y_{12})$ are proportional to frequency, etc.

The final step in this procedure is to apply (7)–(13) to the previous Y parameters in order to determine the values of the SSEC elements. The dependence on frequency of the intrinsic elements obtained in this way is shown in Fig. 6. It can be observed that all of them are frequency independent at least up to 100 GHz, which is far beyond the frequency range of device operation. This means that the proposed SSEC describes correctly the ac behavior of the MESFET for this bias point. In this way, the Monte Carlo method is shown to be a good test to validate a given SSEC up to frequencies that may be difficult to reach in experimental measurements.

The intrinsic elements of the SSEC have been calculated at the same operating point for MESFET's A and C as well. All of them have also been found independent of frequency.

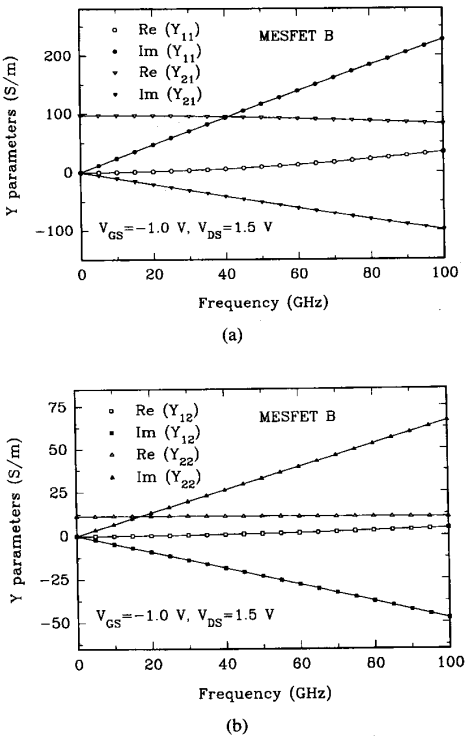

Fig. 5. Real and imaginary parts of the Y parameters corresponding to the bias point $V_{GS} = -1.0\,\mathrm{V}, V_{DS} = 1.5\,\mathrm{V}$ in MESFET B as a function of frequency. (a) Y_{11}, Y_{21}, and (b) Y_{12}, Y_{22}.

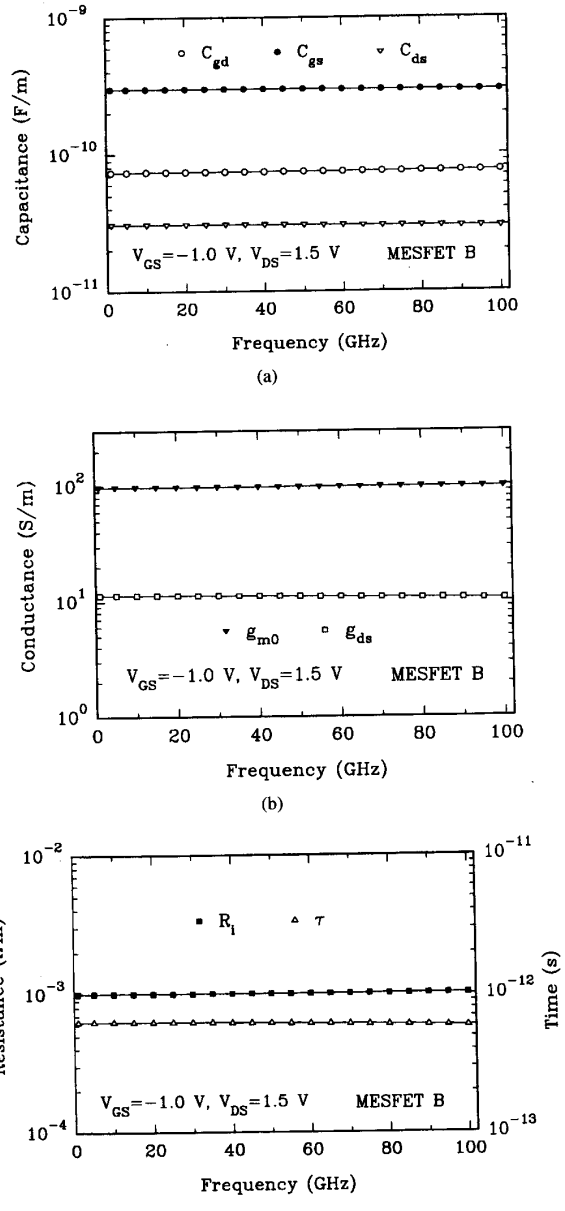

Fig. 6. Elements of the intrinsic small-signal equivalent circuit of Fig. 1 as a function of frequency for MESFET B at the working point in saturation corresponding to $V_{GS} = -1.0\,\mathrm{V}, V_{DS} = 1.5\,\mathrm{V}$. (a) Capacitances, (b) conductances, and (c) intrinsic resistance and delay time.

Their values are given in Table I. It must be pointed out that at $V_{GS} = -1.0$ V, $V_{DS} = 1.5$ V, the drain current is not very high, as can be observed in Fig. 3, due to the fact that nearly all the channel is depleted by the gate voltage. This means that under these conditions the accumulation of carriers between the gate and the drain due to their transfer to the upper valleys is not important. Several significant differences are found among the three MESFET geometries. First of all, the presence of carriers flowing through the substrate in MESFET's B and C makes C_{ds} increase in almost one order of magnitude with respect to MESFET A, and g_{ds} becomes also higher due to the weaker saturation of the current. Moreover, the transconductance decreases considerably. On the other hand, both R_i and τ are lowered by the presence of the substrate, since the source-gate and gate-drain paths become less resistive. From these data, it is confirmed (what is well known) that the presence of the substrate degrades the MESFET performance. When the gate is moved towards the source (MESFET C), some elements change with respect to the case in which the gate is centered (MESFET B). C_{gs} increases and C_{gd} decreases, as corresponds to the shorter and longer distance between the respective electrodes. The nearness between the gate and the source lowers the value of the intrinsic resistance R_i, while the greater gate-drain separation enlarges the transit time between both contacts τ. It is also detected that g_{ds} is slightly lower and g_{m0} higher, what was already expected from the current-voltage characteristics of Fig. 3. In conclusion, the displacement of the gate towards the source improves somewhat the MESFET performance.

The same analysis has been carried out for a bias point with a higher drain current, corresponding to $V_{GS} = -0.5$ V, $V_{DS} = 1.5$ V. The values of the intrinsic SSEC parameters for this point at 5 GHz are given in Table II. As compared with the previous point, an important increase in the transconductance and in the gate-source capacitance is detected, according to the broadening of the active channel. The delay time has increased

TABLE I
VALUES AT 5 GHz OF THE INTRINSIC SMALL-SIGNAL EQUIVALENT-CIRCUIT ELEMENTS AT $V_{GS} = -1.0\,\text{V}, V_{DS} = 1.5\,\text{V}$ IN THE THREE MESFET'S CONSIDERED

MESFET	C_{gd} (10^{-11} F/m)	C_{gs} (10^{-10} F/m)	R_i ($10^{-3}\,\Omega$ m)	g_{m0} (S/m)	τ (10^{-12} s)	C_{ds} (10^{-11} F/m)	g_{ds} (S/m)
A	6.28	3.45	1.43	115.6	0.944	0.46	3.16
B	7.37	2.99	1.00	97.5	0.634	3.07	11.32
C	6.76	3.15	0.89	102.3	0.717	3.07	10.48

TABLE II
VALUES AT 5 GHz OF THE INTRINSIC SMALL-SIGNAL EQUIVALENT-CIRCUIT ELEMENTS AT $V_{GS} = -0.5\,\text{V}, V_{DS} = 1.5\,\text{V}$ IN THE THREE MESFET'S CONSIDERED

MESFET	C_{gd} (10^{-11} F/m)	C_{gs} (10^{-10} F/m)	R_i ($10^{-3}\,\Omega$ m)	g_{m0} (S/m)	τ (10^{-12} s)	C_{ds} (10^{-11} F/m)	g_{ds} (S/m)
A	1.96	5.79	1.06	160.9	1.29	1.26	3.44
B	3.62	5.13	1.11	153.6	1.09	3.92	9.57
C	2.82	5.47	0.98	154.5	1.12	4.02	9.17

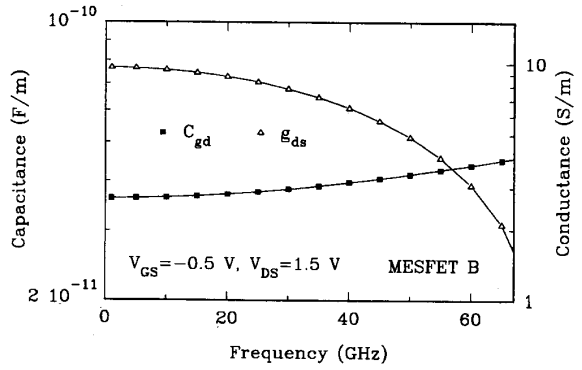

Fig. 7. C_{gd} and g_{ds} at the working point in saturation corresponding to $V_{GS} = -0.5\,\text{V}, V_{DS} = 1.5\,\text{V}$ in MESFET B as a function of frequency.

as well due to the appearance of slow carriers in the upper valleys between the gate and the drain, which leads to a charge accumulation reflected in the substantial decrease of C_{gd} [3].

The frequency dependence of the different elements has also been analyzed. As in the previous bias point, $C_{ds}, C_{gs}, R_i, \tau$ and g_{m0} are nearly constant with frequency up to 100 GHz for the three MESFET's. However, g_{ds} and C_{gd} present the behavior shown in Fig. 7 for the case of MESFET B (a similar result was found for MESFET's A and C). They are strongly dependent on frequency from 15 GHz: g_{ds} decreases as the frequency becomes higher, and C_{gd} increases. This dependence has also been found experimentally [16]. Consequently, the proposed equivalent circuit (Fig. 1) is valid with constant parameters only up to 15–20 GHz for this working point. Both elements, g_{ds} and C_{gd}, are connected with the behavior of the MESFET high-field region: the drain side of the active channel. For $V_{GS} = -0.5$ V a broad part of the channel is not depleted, and an important accumulation of carriers in the L and X valleys takes place at its drain end. In this region the carrier velocity decreases although the field is increasing, what leads to a local negative differential resistance.

It seems clear that the two elements g_{ds} and C_{gd} are not enough to describe correctly the physical effects taking place in the high-field region, which are more pronounced as the length of the gate becomes shorter. Therefore, some changes must be introduced in the equivalent circuit in order to characterize these effects [17], [18]. A plausible modification is to split the external drain series resistance in two contributions: a constant external one, and an intrinsic bias-dependent resistance, which may be positive or negative depending on the operating conditions [16], [17]. The problem in such a case is to derive analytical expressions for the elements of the equivalent circuit.

V. CONCLUSIONS

A Monte Carlo technique for the calculation of the intrinsic elements of the FET SSEC has been described and applied to MESFET's. The method consists in the extraction of the different elements from the frequency-dependent Y parameters of the intrinsic FET, obtained from the Fourier analysis of the device transient response to voltage perturbations at the terminals. For low drain currents under saturation the values calculated for the elements of the SSEC are found to be frequency independent in a broad range. This fact confirms that under these conditions the proposed equivalent circuit describes correctly the ac behavior of the MESFET in the whole frequency range of operation. However, for high drain currents g_{ds} and C_{gd} depend on frequency due to the presence of non-stationary dynamic phenomena in the channel, which could be characterized by the inclusion of a drain intrinsic bias-dependent series resistance in the SSEC.

Three different MESFET geometries and their influence on the results have been analyzed. The presence of a semi-insulating substrate increases considerably both g_{ds} and C_{ds}, while reduces g_{m0}, R_i and τ. In general, the substrate degrades the MESFET electrical performance. When the gate is displaced towards the source, C_{gs}, g_{m0} and τ are increased, while C_{gd} and R_i are reduced, on the whole improving slightly the device performance, mainly at low frequency.

Finally, the Monte Carlo method, which includes all the transport processes relevant to small semiconductor devices, has been shown to be a powerful tool to check the validity of small-signal models up to frequencies that are difficult to reach experimentally. Its only drawback could be the CPU time needed for the simulation of the transients, which in any case is not very long since these are relatively short.

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REFERENCES

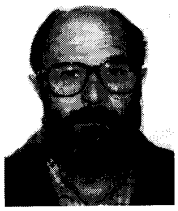
[1] H. Rothe and W. Dahlke, "Theory of noisy fourpoles," *Proc. IRE*, vol. 44, pp. 811–818, June 1956.
[2] S. D. Greaves and R. T. Unwin, "Accurate noise characterization of short gate length GaAs MESFET's and HEMT's for use in low-noise

optical receivers," *Microwave and Optical Tech. Lett.*, vol. 6, pp. 60–65, Jan. 1993.
[3] C. Moglestue, *Monte Carlo Simulation of Semiconductor Devices*. Cambridge: Chapman & Hall, 1993.
[4] S. Iezekiel, "Equivalent circuit modelling," in C. M. Snowden and R. E. Miles (eds.), *Compound Semiconductor Device Modelling*. London: Springer-Verlag, 1993, pp. 149–169.
[5] H. Fukui, "Determination of the basic device parameters of a GaAs MESFET," *Bell. Syst. Tech. J.*, vol. 58, pp. 771–797, Mar. 1979.
[6] R. A. Minasian, "Simplified GaAs MESFET model to 10 GHz," *Electron. Lett.*, vol. 13, no. 8, pp. 549–551, 1977.
[7] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Technol.*, vol. MTT-36, pp. 1151–1159, July 1988.
[8] M. Berroth and R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Technol.*, vol. MTT-38, pp. 891–895, July 1990.
[9] F. Diamont and M. Laviron, "Measurement of the extrinsic series elements of a microwave MESFET under zero current condition," in *Proc. 12th European Microwave Conf.*, 1982, pp. 451–456.
[10] T. González, D. Pardo, L. Varani, and L. Reggiani, "Monte Carlo simulation of electronic noise in MESFET's," in *Proc. 1994 Gallium Arsenide Applications Symposium (GAAS 94)*, Torino, Italy, Apr. 1994, pp. 385–388.
[11] V. Gruzinskis, S. Kersulis, and A. Reklaitis, "An efficient Monte Carlo particle technique for two-dimensional transistor modelling," *Semicond. Sci. Technol.*, vol. 6, pp. 602–606, 1991.
[12] S. E. Laux, "Techniques for small-signal analysis of semiconductor devices," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 2028–2037, Oct. 1985.
[13] C. Jacoboni and P. Lugli, *The Monte Carlo Method for Semiconductor Device Simulation*. Vienna: Springer-Verlag, 1989.
[14] T. González, J. E. Velázquez, P. M. Gutiérrez, and D. Pardo, "Five-valley model for the study of electron transport properties at very high electric fields in GaAs," *Semicond. Sci. Technol.*, vol. 6, pp. 862–871, 1991.
[15] M. B. Patil and U. Ravaioli, "Transient simulation of semiconductor devices using the Monte-Carlo method," *Solid-State Electron.*, vol. 34, pp. 1029–1034, 1991.
[16] J. Portilla, M. Campovecchio, R. Quéré, and J. Obrégon, "A new coherent extraction method of FET's and HEMT's models for MMIC applications," in *Proc. 1994 Gallium Arsenide Applications Symp. (GAAS 94)*, Torino, Italy, Apr. 1994, pp. 377–380.
[17] Y. K. Feng, "An approach to determine the small-signal equivalent circuit of sub-mm GaAs MESFET's including effects of nonstationary electron dynamics," *Solid-State Electron.*, vol. 36, no. 3, pp. 443–453, 1993.
[18] H.-O. Vickes, "Determination of intrinsic FET parameters using circuit partitioning approach," *IEEE Trans. Microwave Theory Technol.*, vol. MTT-39, pp. 363–366, Feb. 1991.

Tomás González was born in Salamanca, Spain, in 1967. He graduated in physics from the University of Salamanca in 1990, where he received the Ph.D. degree in physics in 1994.

Since October 1990, he has been working with the Electronics Group in the Department of Applied Physics at the University of Salamanca, with a Grant from the Spanish Education Ministry. In the Fall of 1992 he was working in the Department of Physics at the University of Modena, Italy. In 1994, he became Temporary Associate Professor. His research interests include the characterization of noise processes in semiconductor materials and devices by means of Monte Carlo method, and the analysis of the ac behavior of electronic devices, with special application to III-V materials.

Dr. González received the ESSDERC'93 Best Student Paper Award.



Daniel Pardo was born in Valladolid, Spain, in 1946. He graduated in physics in 1971 from the University of Valladolid, where he also received the Ph.D. degree in 1975.

From 1971 to 1981, he worked in the Department of Electronics at the University of Valladolid on the characterization of semiconductor materials and modeling of semiconductor devices, and was promoted to Associate Professor in 1978. In 1981, he joined the Department of Applied Physics at the University of Salamanca, where he has been Full Professor since 1983, as well as Head of the Electronics Group. His current research interest is the Monte Carlo simulation of semiconductor devices with special application to noise characterization.