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Nonlinear electron properties of an InGaAs/InAlAs-based ballistic deflection transistor: Room temperature DC experiments and numerical simulations

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ABSTRACT

We present a detailed experimental and numerical study of a novel device so-called ballistic deflection transistor (BDT). Based on InGaAs–InAlAs heterostructure on InP substrate, BDT utilizes a two dimensional electron gas (2DEG) supported by a gated microstructure to achieve nonlinear electron transport at room temperature. BDT channel is larger than the mean free path implying that electron transport is not purely ballistic in nature. However, the asymmetric geometrical deflection combined with the electron steering caused by the applied differential gate voltages ultimately results in an attractive nonlinear behavior of the BDT useful for the working of the large scale devices at room temperature. Device performance was studied by analyzing the effects of several modifications of the BDT geometry and biasing conditions, both experimentally and by numerical simulations.

1. Introduction

The need for advanced technologies for high end applications like high bandwidth, low delay, low power applications and ultra-high speed computing, is growing as present conventional Si CMOS technology is on the verge of potential saturation. Further scaling of silicon CMOS current devices will lead to a dramatic increase in sub-threshold, gate and reverse biased junction band-to-band-tunneling leakage. All of these lead to deterioration in the device performance and power efficiency [1]. This has prompted increasing research in exploring alternative and unconventional devices such as carbon nano-tube transistors, single electron transistors and graphene based transistors [2] to name few.

The recent and fast advancements in technological process assisted in realizing devices with active regions shorter than the mean free path of electrons, thus, facilitating ballistic transport, even at room temperature (RT). In this context, in recent years great efforts have been made to fabricate and characterize new nanometer-size electronic devices with ingenious geometries, in which electrons move ballistically unhindered by collisions with the lattice defects, impurities and phonons and path is largely determined by specular reflection from tailor-designed device boundaries [3]. Related to this, for the first time in 1992 Palm and Thylen [4] presented a novel concept of electrons deflected by a transverse field in a Y-branch switch. In 1998 Song et al. [5] proposed a first GaAs/AlGaAs based ballistic rectifier at cryogenic temperature. In 2000, Hieke et al. demonstrated the first ballistic rectification operation [6] and presented a Y-branch switch with lateral gates [7] both at RT. Xu theoretically predicted the nonlinear transport in T-branch junctions (TBJ) [8]. Pronounced asymmetries of electrical properties are observed in nanoelectronic, symmetric GaAs/AlGaAs Y-branches in 2001 [9]. In 2001 Shorubalko et al. [10] published experimental results on nonlinear electrical properties of InGaAs/InP based TBJ. A nano-scale unipolar rectifying diode called Self-Switching Diode (SSD) has also been recently proposed in [11]. All of these devices exhibit nonlinear effects and can operate at higher frequencies even at RT. In fact, the estimated electron velocity in these III–V materials is about 10^8 cm/s, which is 10 times faster than in silicon. Hence, smartly tailored transistor designs can be implemented using these technologies to exploit such speed. In fact, intrinsically, based on Monte Carlo simulations ballistic nano-devices are known to operate up to 1 THz frequencies [12]. However, there is no real solution yet to reduce the parasitic effects. Therefore, in experiments these types of devices are proved to work at 50 GHz for the ballistic rectifier [13], at 94 GHz for detection in YBJs [14] and up to 110 GHz in another new type of device so-called Self-Switching Diode (SSD) [15], but remarkably all at RT. Most recently, Irie

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et al. has experimentally claimed a RT TBJ operation up to 500 GHz, when excited by picosecond electrical pulses [16]. The applications of these nano-devices are manifold: rectification, frequency doubling, phase detection, Boolean logic functionalities, signal detection, etc. For instance, it is possible to design logic circuitry as it is proposed theoretically in [17,18] and experimentally verified for example: frequency doubling [19], NAND gate [20], set-reset latch [21], NOR gates [22], half-adder with small number of interconnected Y-junctions [23], or with TBJs and YBJs controlled by Schottky wrap gates (WPGs) [24]. Most important from the end-user point of view is that all the above devices are operated at RT.

In the same context, recently our group proposed a novel device so-called ballistic deflection transistor (BDT) [25]. BDT is a novel InGaAs/InP-based device in which electrons can move ballistically, guided by strategically defined shapes, edges and inner obstacles, through tailor-designed geometries. Electron steering, ballistic deflection and channel pinch-off are the three major effects, which define the transport inside BDT. BDT is entirely different from the conventional transistors as no doping junction or barrier structure is employed. Because of the small feature size, and low parasitic capacitances, BDT has the ability to operate at high frequencies [25]. In addition, this device can be used to construct logic applications [26]. The aim of this paper is to optimize the nonlinear performance of BDT by an extensive study based on the geometrical parameters and bias conditions using both room temperature DC experiments and numerical simulations.

The paper is organized as follows. In Section 2, a brief overview of BDT is presented, in which its heterostructure and fabrication process is described which is followed by a description of its principle of operation using non-Ohmic behavior study. Section 3 describes the experimental DC characterization in which geometrical and bias dependence of BDT performance is studied with respect to the presence of significant architectural features like the deflector, its sizing and various dimensional ratios. In Section 4, BDT optimization is explained using hydrodynamic (HD) simulations where trench width are optimized for maximum performance and channel width is studied. Finally, Section 5 summarizes the results of this study and concludes the paper.

2. BDT overview

2.1. Heterostructure and fabrication process

Fig. 1a shows the layer structure of the wafer grown using Molecular Beam Epitaxy (MBE). It consists of lattice matched layers of InGaAs and InAlAs on an InP substrate. The layers consist of a 450 nm InAlAs buffer, a 50 nm InGaAs channel, InAlAs spacer of L_s = 20 nm thickness followed by a planar silicon δ-doped ($N_\delta = 2 \times 10^{12}$ cm^{-2}) InAlAs layer, a 30 nm Schottky barrier and finally a 10 nm InGaAs undoped cap layer. 2DEG resides along the interface of 20 nm InAlAs spacer and 50 nm InGaAs channel. The value of L_s and N_δ must be adjusted to enhance the electron sheet density without degradation of the mobility. An interesting experimental trade-off for ballistic applications between these magnitudes is presented in [27]. For $In_xGa_{1-x}As$ with high Indium content ($x > 70\%$), the mean free path is about 6 μm, 1–2 μm and typically around 140 nm for 4.2 K, 77 K and 300 K respectively [3]. That is why the mean free path in the 2DEG, even at RT, can be longer than the active region of the nano-device. This heterostructure is similar to the High-Electron Mobility Transistors (HEMTs), therefore, it offers the advantage of joint integration resulting in an extension of the already demonstrated sub-millimeter frequency applications of HEMTs [28]. The measured RT mobility μ and electron sheet density n_e of 2DEG were 1.1×10^4 cm^2/Vs and 1×10^{12} cm^{-2}, respectively.

For the realization of a particular geometry of BDT, a two step electron beam lithographic technique is used. Fig. 1b shows SEM image of the device realized with this technique. For the first step of fabrication, a positive resist 950 K PMMA (~100 nm) is spun over a 50 nm carbon hard mask before doing the electron-beam lithography. After writing the pattern and stripping off the resist, ion-mill etching was done to define the active region of 2DEG layer. The resulting mesa typically has a step height of 130 nm so that all the layers above InAlAs buffer were completely etched away. After that, for the second step of fabrication, the electron-beam lithography is used again to pattern the Ni/Ge/Au Ohmic contacts by successive metal layer deposition and forming gas annealing at 420 °C for 30 s. The metal layer thickness and the annealing temperature have been optimized, giving an acceptably low contact resistance (~0.5 Ω mm) on every run. In future works, a doped cap layer will be included to improve the quality of the contact resistances. Finally, Ti/Au probe pads are patterned and deposited by usual lift-off technique.

2.2. Principle of operation

A more detailed top-view SEM image of BDT with bias conditions is shown in Fig. 1b. It can be seen that BDT has six voltage terminals: a grounded electron source (V_{SS}), left and right gates (V_{LG} and V_{RG}), and three biased drains (V_{TD}, V_{LD} and V_{RD}). The top drain is a pull-up terminal which pulls electrons towards upwards to accelerate electrons while left and right drains are output terminals. Device symmetry is maintained along V_{SS}–V_{TD} axis but device is asymmetric along V_{LD}–V_{RD} axis, which contributes towards the nonlinearity of BDT. A DC experimental transfer characteristic of BDT is shown in Fig. 2, where the dependence of I_{LD} and I_{RD} on voltage applied at the gates in a push–pull bias fashion ($V_{LG} = -V_{RG}$) is shown. The voltages applied in the drains are: $V_{LD} = V_{RD} = V_{TD} = 1$ V. From Fig. 2, we observe that I_{LD} first increases as a function of gate voltage then decreases. The difference in amplitude of I_{LD} and I_{RD} occur due to the process variations in trenches widths (t) and output channels widths (c) (Fig. 1b). This increase and decrease in the current with gate voltage is due to the channel first is pinched off, then, as the gate voltage is increased, the electrons are steered from the right drain into the left drain, and, eventually, the channel pinches off again. Note that the pinch-off gate voltage is the voltage defined when current starts decreasing. Three key effects in BDT are the gate control steering effect, deflector re-direction effect and channel pinch-off effect. Steering effect comes into picture when electrons experience a lateral field generated by gate bias which steers them to either left or right. Re-direction effect occurs when physical encounter between deflector and electrons helps electrons to move either towards right or left drain channels, depending on the side of the deflector where collision happens. Pinch-off can be observed when a strong bias depletes the channel completely. At the peak between the steering region and the pinch-off region, we have the maximum conductivity. The positive and negative transconductance regions on the characteristics, enable designing circuits that are either inverting or non-inverting, depending only on gate offset voltage. Also, the shape of the transfer characteristics makes the BDT a frequency doubler. A gate bias that enables the input to swing past either side of the peak output current will result in an output signal that is twice the input frequency. A sophisticated Monte Carlo simulation has proved this efficiency up to 200 GHz [29]. In the inset of Fig. 2 variation in the left gate leakage current with gate voltage is shown where the value is one order of magnitude less than the output current.

Concerning the possible logic applications of the BDT, inset of Fig. 2 shows two different gate bias conditions and electrons trajectories. A simple operational mechanism of BDT can be explained as follows: when the electron current moves along the right drain,

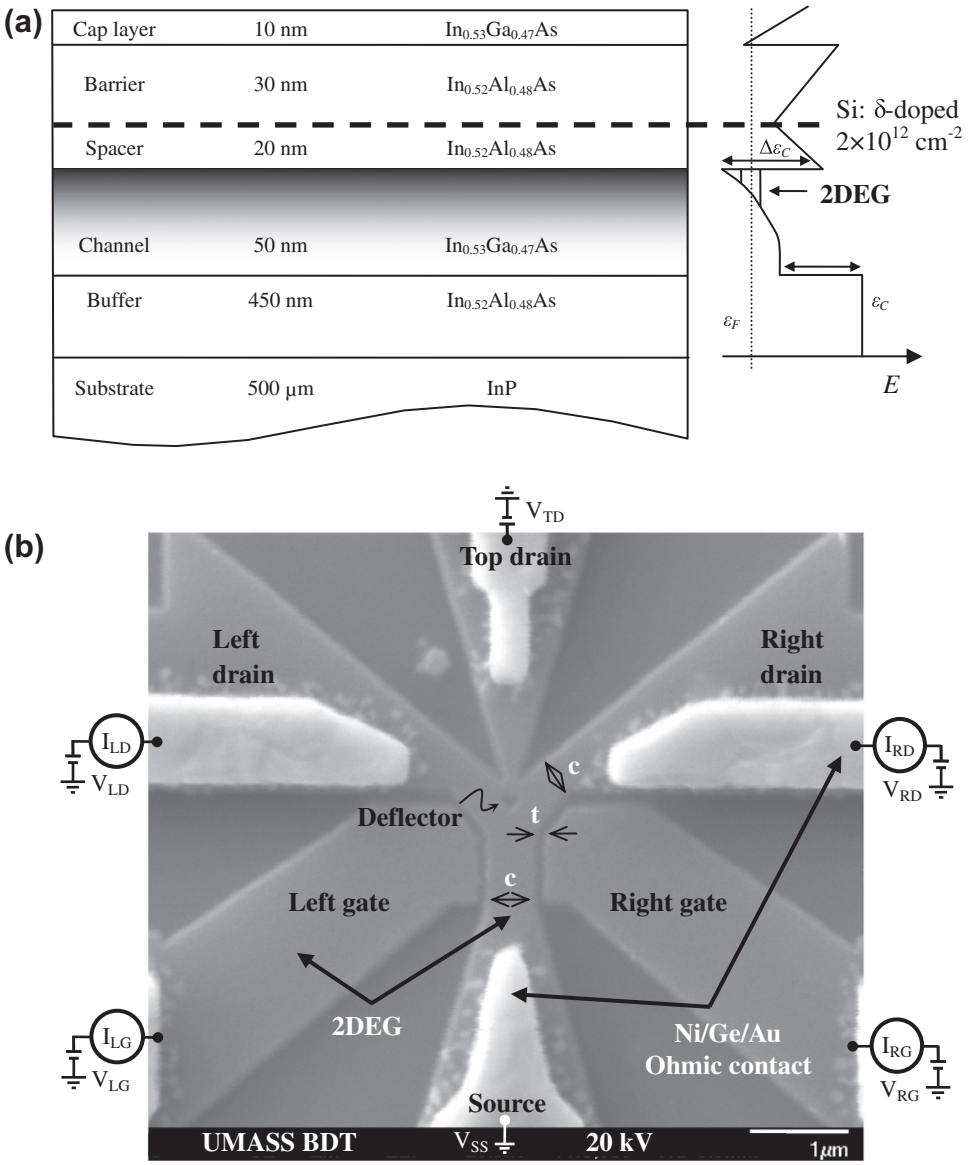

Fig. 1. (a) The stacked layers used for the wafer and physical conduction band aspect including 2DEG. (b) SEM image of the top-view of a BDT is pictured including ohmic contacts. Channel width c = 500 nm gates and trench width t = 120 nm. The top-left and top-right ports are drain ports (V_{LD} and V_{RD} respectively), bottom-left and bottom-right ports are gates (V_{LG} and V_{RG} respectively), top port is a bias port (V_{TD}) which is a pull-up terminal, and the bottom port is the source (V_{SS}). The bright area represents the 2DEG and the dark regions including the triangle region is where the material has been removed from the 2DEG structure. 2DEG has high electrical conductivity whereas dark areas are non-conductive.

transistor registers logic "1" at right drain and logic "0" at left drain and vice versa. It is this intrinsic logic behavior of the device that makes it attractive. The usefulness of the device for high speed data processing is possible after resolving issues such as interconnections, fan-out, parasitic capacitance and interfacial traps, which are predominant in planar devices like BDT. In spite of these challenges, the inherent properties associated with such kind of devices can assist in achieving promising performance.

2.3. Theoretical explanation and nonlinear behavior

The idea of BDT was developed from the nonlinear RT ballistic rectifier proposed by Song et al. [5], where a small-amplitude AC current runs back and forth across a 100 or 200 nm device, producing a DC voltage drop from top to bottom, as the electrons hit the triangular deflector. Our group added gates to Song's ballistic rectifier, thereby turning it into BDT as shown before. For a small scale device and at low temperatures, coherent transport description based on the Landauer–Büttiker theory [30] is well suited. The exploratory Landauer–Büttiker formalism for purely ballistic BDT is explained below [31].

The V_{RD} vs I_{RD} characteristic from [3] is given by

$$R_{RD} = \frac{V_{RD}}{I_{RD}} \tag{1}$$

where I_{RD} is the current in the right channel and V_{RD} is the voltage induced in right channel.

At equilibrium when no biasing is applied,

$$T_{LD\leftarrow SS} = \int_{-\pi/2}^{0} (N_{SD}/2)\cos\theta d\theta \tag{2}$$

$$T_{RD\leftarrow SS} = \int_{0}^{\pi/2} (N_{SD}/2)\cos\theta d\theta \tag{3}$$

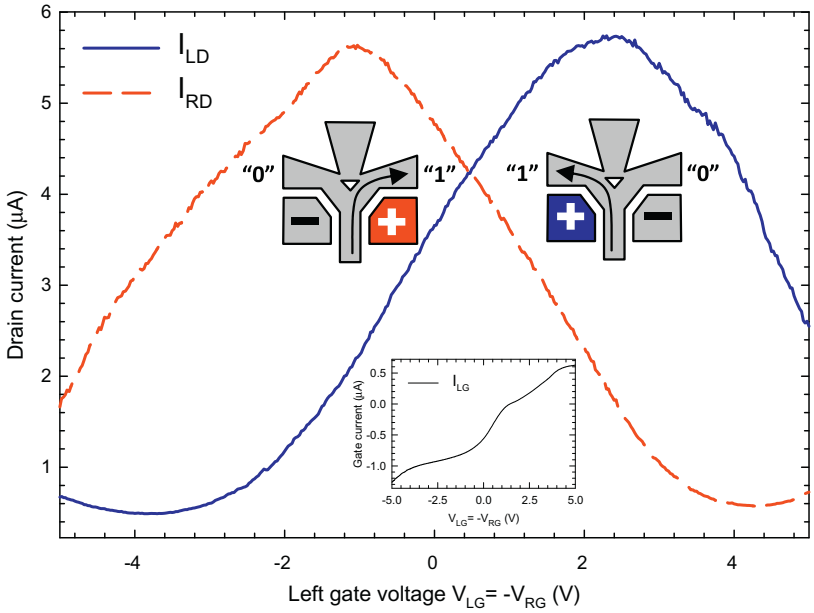

Fig. 2. Typical transfer characteristic of BDT as a function of push–pull gate voltage in reference to the left gate. Inset: Gate leakage I_{LG} vs V_{LG} and schematic showing electrons trajectory for negative and positive left gate bias conditions.

where N_{SD} is the number of conducting modes in bottom channel. θ is the angle made by the injected electron with the V_{SS}–V_{TD} axis. When gates and drains biasing are applied, transmission will be dominant on the positive gate bias region. Thus transmission coefficients $T_{LD\leftarrow SS}$ and $T_{RD\leftarrow SS}$ will depend on the gate polarity. Therefore, when the right gate and injection angle of electrons into the bottom channel is positive, the right drain transmission will be defined as,

$$T_{RD\leftarrow SS}(bias) - T_{RD\leftarrow SS}(eq) = (N_{SD}/2)(\sin\theta_e - \sin\theta_0) \tag{4}$$

$$T_{LD\leftarrow SS}(bias) - T_{LD\leftarrow SS}(eq) = -(N_{SD}/2)(\sin\theta_e - \sin\theta_0) \tag{5}$$

where

$$\theta_e = \theta_0 + \arcsin\left[\frac{\Delta v}{v_F}\sin\theta_0\right] \tag{6}$$

where θ_0 be the minimum angle for an electron ejected from source to encounter scattering with deflector, Δv is the drift velocity and v_F is Fermi velocity. In above equations, it can be seen that the $T_{RD\leftarrow SS}$ is positive, since we are dealing only with the right drain transmission. At the same time, for left drain, $T_{LD\leftarrow SS}$ will be negative. Thus using above equations,

$$R_{RD} = \frac{V_{RD}}{I_{RD}} = \frac{3h(\sin\theta_e - \sin\theta_0)}{e^2 N_{TD}[2N_{RD} - 3N_{TD}(1-\sin\theta_0)^2]} \tag{7}$$

For small currents, above equation reduces to

$$V_{RD} = -\frac{3\pi h^2}{4e^3 N_{TD} E_F N_{RD}} I_{RD}^2 \tag{8}$$

for electrons that are directed toward the right drain and

$$V_{LD} = -\frac{3\pi h^2}{4e^3 N_{TD} E_F N_{LD}} I_{LD}^2 \tag{9}$$

for the electrons which are directed towards the left drain. I_{LD} is the current in the left channel, E_F is the Fermi Energy, h is the Planck's constant, e is the electronic charge, N is the number of conducting modes (*LD* for left drain, *RD* for right drain, and *TD* for the top drain).

If we sum V_{RD} and V_{LD} we get a net potential between the two drains. With both gates at an equal voltage (symmetric gate conditions), V_{RD} and V_{LD} are equal. However, as the gates become asymmetric, due to the unequal width opening of the right/left branches, an asymmetric carrier injection into them leads to change in the current in each channel and therefore a potential difference increases nonlinearly. From Eq. (8), we can investigate that when the right gate is positive, the right conducting channel opens, which increases the number of conducting modes (N_{RD}) and the right channel current (I_{RD}), which changes V_{RD}. At the same time, the left gate is negatively biased which depleted the left conducting channel and reduces the number of left channel conducting mode (N_{LD}) and left channel current (I_{LD}), which changes V_{LD}. Hence, this mechanism helps in increasing the nonlinearity in addition with the deflector scattering mechanism where deflector directs electrons away from the center drain port.

This Landauer–Büttiker formalism has been used to explain various nonlinear transport phenomena as explained in [3] such as quantized conductance in a point contact, electron focusing experiments, negative bend resistance, quenched and negative Hall effects, and lateral hot ballistic electron devices, but only at low temperatures and in purely ballistic devices. However, in our case where the devices are bigger and not strictly ballistic rather quasi-ballistic or diffusive, the coherence phenomena and quantum effects such as energy quantization play no significant role at RT. In addition, this theory cannot assist in studying the geometry and their effects on the device performance. Therefore, in our opinion, at RT, it is not the ballistic transport, but the device asymmetry, which causes device to work. To corroborate this hypothesis, we performed an experiment to replicate the nonlinear behavior proposed in the Song's rectifier [5] by removing the gate biasing in our BDT as shown in the inset of Fig. 3. When biasing left and right branches in push–pull fashion, $V_{LD} = -V_{RD} = V = 0.5$ V electrons hit the center obstacle, and then they are deflected downward. The potential difference between the bottom and the top branches of the device, $V_{BT} = V_B - V_T$ is shown in Fig. 3. It can be seen that for a bigger device of channel width $c = 400$ nm, the output voltage is smaller as compared to the one with a channel width $c = 200$ nm. It implies that for large devices, although the

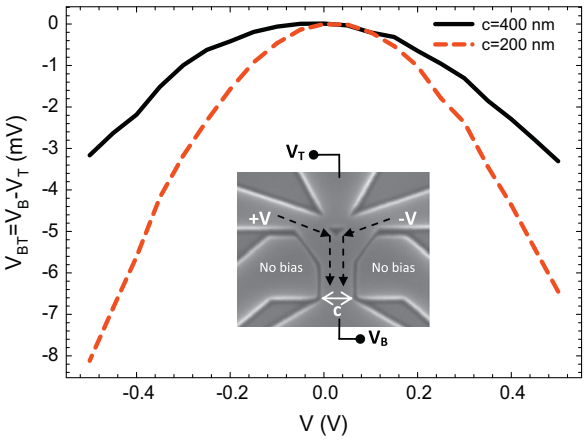

Fig. 3. Room temperature potential difference between the bottom (V_B) and top branches (V_T), $V_{BT} = V_B - V_T$, as a function of V when biasing the left and right branches in push–pull fashion. Inset: SEM image of a BDT operating as a ballistic rectifier [7] because gates are not biased.

rectification behavior is weaker, the nonlinearity still exists at RT. It is also mentioned in [32–34] that even for large YBJ devices of several micrometer central junction sizes, which is much larger than the mean free path of electrons in the material, the nonlinear electrical properties can be observed.

3. DC experimental measurements

Since the electron scattering with the designed device boundaries is one of the main factors in the working principle, we assume that there is an inevitable impact of the device geometry on the BDT performance. Therefore, by simply tailoring the topology of the device, the electron transport can be optimized and controlled in order to enhance its performance. It is to be noted that our BDT is a large device and the channel length is larger than the electron mean free path. In this regime, the transport is certainly not purely ballistic but rather quasi-ballistic or diffusive, but, interestingly the billiard model still applies, particularly in reference to the principle of deflection. While studying BDT, following criterions such as deflector sizing, dimensional ratios and bias conditions were taken into account. The schematic sketch of our BDT is shown in Fig. 4 showing various important geometrical parameters: c = channel width, a = top drain opening, b = deflector width, t = trench width, h = deflector height, s = distance between channel edge and deflector, and k = position of the deflector. It is to be noted that the full height of the device is constant (970 nm). It means that when we change the k, and since h is constant, the distance between the top drain opening and the deflector will change accordingly.

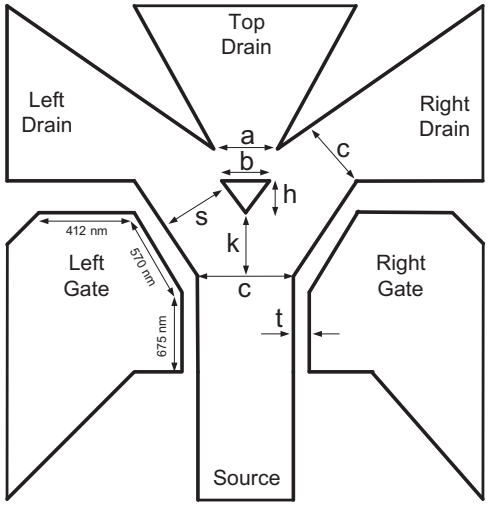

Fig. 4. Schematic of a specific geometry of BDT showing different parameters and dimensions. The values of k, a and s will be optimized using experimental measurements whereas b, h and t will be studied by means of ATLAS simulations. The full height of the central region is constant.

First, experimentally, we performed detailed study to optimize the performance of BDT for higher output current and low top drain leakage in accordance to the presence of the deflector and the parameters a, s and k while keeping c = 500 nm, b = 500 nm, h = 350 nm and t = 120 nm constant. Optimized BDT architecture is then used to characterize the device at different drain bias conditions.

3.1. BDT performance dependence on geometry

As the size of electronic devices is reduced, the surface/volume ratio increases considerably and, in strong contrast to conventional devices, when dimensions reach the nanometric scale, dimensional effects can get to have a remarkable importance on electron transport. The role and the influence of geometry on the output characteristics thus become decisive. So, in this section we study the effect of the deflector and dimensional ratios on the performance of the BDT. The set up for the DC experiments which are performed at RT is the same as explained in Fig. 1b. A push–pull gate sweep is applied, $V_{LG} = -V_{RG}$ from 0 to ± 5 V, and each drain was kept at the same bias, $V_{RD} = V_{LD} = V_{TD} = 1$ V.

3.1.1. Presence of deflector

Deflector is one of the most significant structures in BDT. It breaks the symmetry of the device with respect to $V_{LD} - V_{RD}$ axis. The size of the deflector in actual device is much larger than the Fermi wavelength λ_F of the conducting electrons and comparable to their elastic mean free path. Therefore, the physical collision between deflector and electrons will redirect electrons effectively. This should produce an effect similar to the ballistic bridge rectifier [5]. Its placement in 2DEG channel is therefore an important parameter to study.

To investigate the importance of deflector in the performance of BDT, an experimental comparison of BDT with and without deflector is performed and plotted against the push–pull gate voltage in Fig. 5a. Also the top drain current is shown in Fig. 5b. In this case, a = 400 nm, k = 420 nm and s = 665 nm are chosen. We noticed that I_{LD} is more and I_{TD} is less in case of BDT with-deflector as compared to the one without-deflector, which explains that deflector is required to increase the output. It is also observed that although I_{LD} was higher in with-deflector case, the difference in I_{LD} for with and without deflector response is not very significant. This is due to the strong steering effect produced by the gate voltages, which controls electrons to conduct along the vicinity of gates resulting into steering towards right or left drain channel depending on the gate polarity. This experiment signifies that the presence of deflector is imperative for better performance and reduced leakage.

3.1.2. Dimensional ratios and their effects: k, a and s

In order to study performance comprehensively, we designed and fabricated BDTs with deflector at different positions k keeping a = 400 nm and s = 665 nm. Using same biasing condition as described above, we noticed from Fig. 6a and b that the device performs best when the position of the deflector is k = 420 nm. The difference between left output and leakage is maximum for this value of k = 420 nm. Placing deflector above or below k = 420 nm, reduces the output and increases the leakage. For lower k values

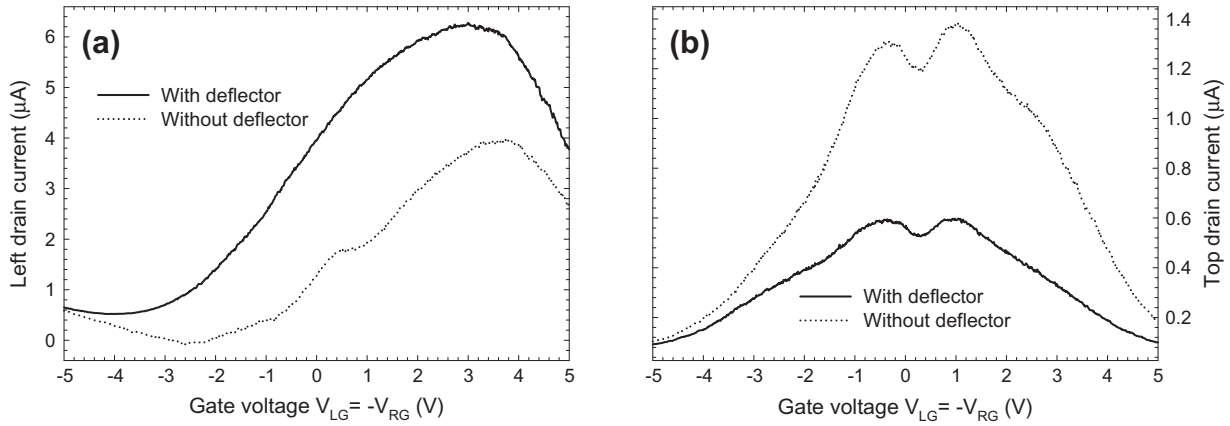

Fig. 5. Experimental influence of the presence or absence of the deflector on the (a) output left drain current I_{LD} and (b) top drain leakage I_{TD}. In case of BDT with deflector, the pinch-off voltage is 3 V, which is smaller than the 3.8 V pinch-off voltage of BDT without deflector. Deflector is important to redirect the electron to either side of the device depending on the gate polarity and to reduce the top drain leakage.

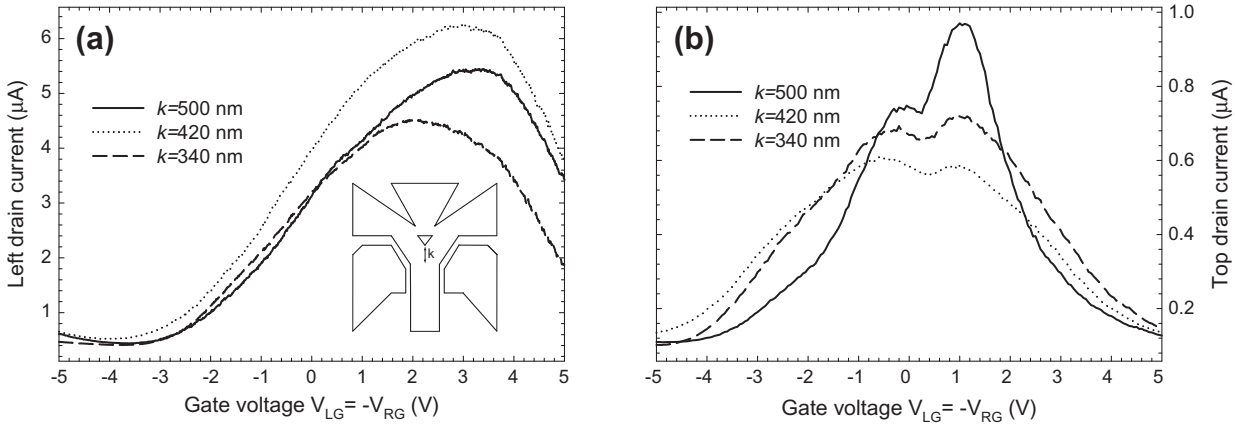

Fig. 6. Experimental influence of the defector position parameter, k on the (a) output left drain current I_{LD} and (b) top drain leakage I_{TD}. For lower k values output current reduces and early pinch-off is observed. I_{LD} is maximum and I_{TD} is minimum for k = 420 nm.

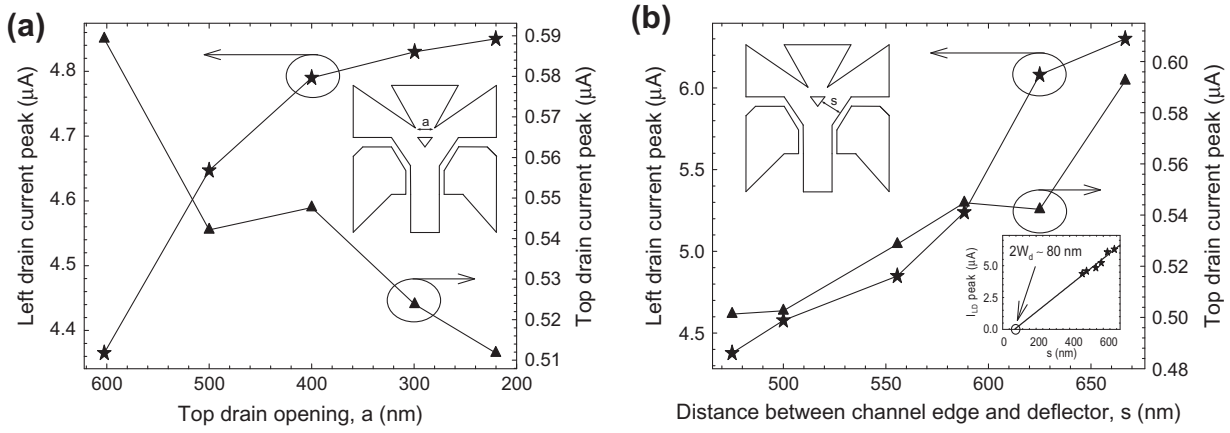

Fig. 7. Variation in left drain current and top leakage current, I_{LD}, I_{TD} with (a) top drain opening, a (s = 550 nm and k = 420 nm) and (b) distance between channel edge and deflector, s (a = 400 nm and k = 420 nm). Inset: estimation of a lateral depletion width $W_d \approx 40$ nm which is consistent with the experimental values reported in Ref. [24] for $In_{0.7}Ga_{0.3}As$ channels.

output current reduces and early pinch-off is observed. This is because when deflector is located at this position, the deflector redirection phenomenon helps gate steering to pinch-off the channel at relativity smaller gate voltages.

Also, two different sets of BDTs of different geometry and sizes were fabricated. The sets are devices with different a and s values. Fig. 7a shows a variation in I_{LD} with a. Note that here s chosen is 550 nm (not optimized yet) and k = 420 nm (optimized) remains

constant. The results indicate that the I_{LD} first rises with the reduction in the value of a and then saturates at $a = 400$ nm. We also note that the change in output current with a is steeper for higher values of a which indicates that the effect of small variations in larger a values is higher. In principle, increase in a means a wider passage to electrons where they can move under a high electric field towards the top drain which increases I_{TD} and vice versa. Majority of electron concentration move towards left and right drain causing increase in I_{LD} and I_{RD}, respectively, when a is smaller. However it is to be noted that increase in parameter a reduces the parameter c of left branch (all the other parameters were kept constant), thereby increasing the resistance of left branch and reducing I_{LD}. However, a negligible change in I_{TD} with increase in a is perhaps due to the presence of the lateral depletion, as a result the top channel nearly pinches off between the top branch edge and the corner of the deflector (gap of 200 nm in this particular case). Secondly, in Fig. 7b, it is shown that I_{LD} and I_{TD} increases with s. Note that here $k = 420$ nm (optimized) and a is chosen as 400 nm because output saturates at this value and if we further reduce a the top drain pull-up effect becomes insignificant. Increase or decrease in s means opening or closing of the channel respectively. As s increases, the performance of BDT is enhanced because of the increase in conducting channel area, which increases the carrier concentration resulting into higher I_{LD} and I_{RD} values with a negligible increase of I_{TD}. So, the value of $s = 665$ nm is selected for further study as it gives the maximum output current. In the inset of Fig. 7b it can be seen the extrapolated I_{LD} value becomes zero at $s \approx 2 \times W_d$ i.e. 80 nm which is consistent with standard lateral depletion of $W_d \approx 40$ nm for InGaAs [35].

3.2. BDT performance dependence on drain bias

With above proposed optimization our large scale BDT device to study the bias dependence will have following parameters: $c = 500$ nm, $k = 420$ nm, $a = 400$ nm, $s = 665$ nm, $b = 500$ nm, $h = 350$ nm and $t = 120$ nm. The current response for a series of drain voltages $V_{RD} = V_{LD} = V_{TD}$ (=1, 0.75, 0.5 and 0.25 V), as a function of gate bias is show in Fig. 8a. One can notice that the drain current increases as a function of applied bias. The increased drain bias causes to strengthen the lateral electric field inside the channel. This control accelerates electrons towards the deflector, which eventually directs them towards right or left channel depending on the gate bias. It can be seen that for the same change in V_{LG} the increase in I_{LD} is more pronounced for higher drain biases, which clearly indicates that the transconductance increases with the drain bias [37]. The top drain leakage current plotted in Fig. 8b also exhibits a strong dependency on the drain bias and increases with it. This is due to the high electron pull towards the top drain and it implies that there is a trade-off between the output current and the top drain leakage. The observed small dip in I_{TD} at $|V_{LG}| < 0.5$ V can be explained in terms of the electrons moving directly towards the center of the deflector, thereby increasing the possibility of bouncing off the electrons in the absence of any significant steering effect.

4. Modeling and simulations

For devices where architecture is imperative for high speed performance, simulation tools constitute a valuable alternative to the expensive and time consuming error procedure. As we explained in Section 2.3, Landauer–Büttiker is suitable for small scale devices at low temperature, so a different approach is imperative to explain the behavioral transport in large scale devices at RT. To support this, various modeling tools and numerical simulations have been employed for similar nano-devices studies. For example a multipurpose billiard model simulator [36], based on classical mechanics of electrons at the Fermi level even being a successful model for the study of BDT, is over simplified. Monte Carlo (MC) simulations based on a semi-classical transport description were able to describe qualitatively the main features of the measured nonlinear effects in BDTs [37] and TBJs [38]. However, the MC algorithms encounter serious difficulties when applied to the extreme conditions occurring in the advanced semiconductor devices. In addition to MC, non-local transport effects, due to the large longitudinal fields and by partially ballistic transport, can be assessed by the use of sophisticated transport models, such as the Energy-Balance (EB) [39] or Hydrodynamic (HD) [40] model. Within HD transport simulations, the non-local transport phenomenon such as velocity overshoot, dependence of mobility on carrier energy or temperature can be taken into account, which will assist the study of nonlinearity in large BDTs in terms of the broken device symmetry. Therefore, in addition to the experimental study, HD simulations will be employed here to examine the performance dependency on its architecture and geometry.

For HD simulations the commercial software simulator ATLAS has been used [41]. We employ a layout approach similar to the one adopted by Mateos et al. [38] in a MC tool to simulate a real 3D device into a 2D simulator. Similar ATLAS modeling has been used in [42] to study Y-branch junctions at RT. Two different types of simulations were performed namely front-view (FV) and top-view (TV) as shown in Fig. 9. For FV simulations, a layered heterostructure was simulated where a delta layer of $\delta = 2 \times 10^{12}$ cm^{-2}

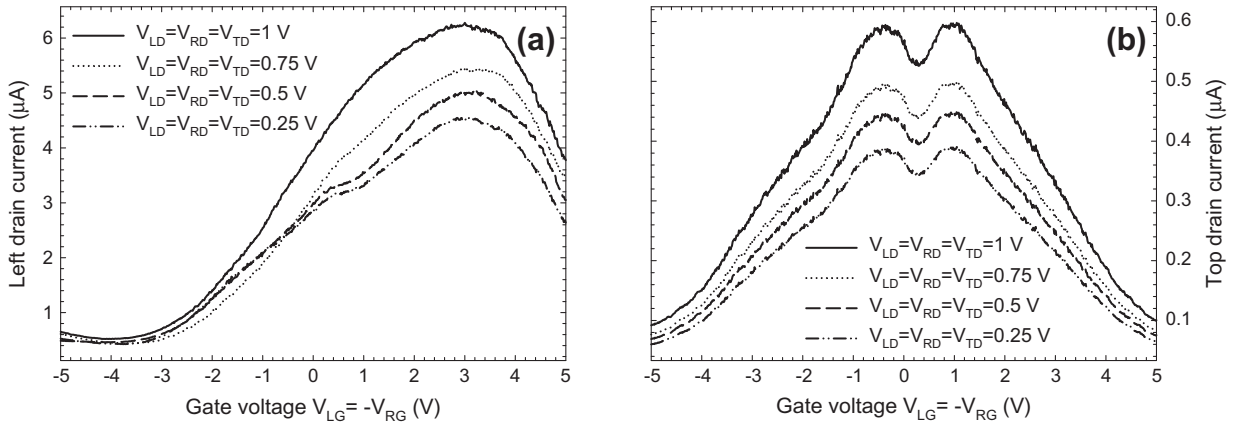

Fig. 8. Experimental influence of the drain bias $V_{LD} = V_{RD} = V_{TD}$ on the (a) output left drain current I_{LD} and (b) top drain leakage I_{TD}. Both, I_{TD} and I_{LD} increase with drain bias. Also the difference between the current level increases with bias.

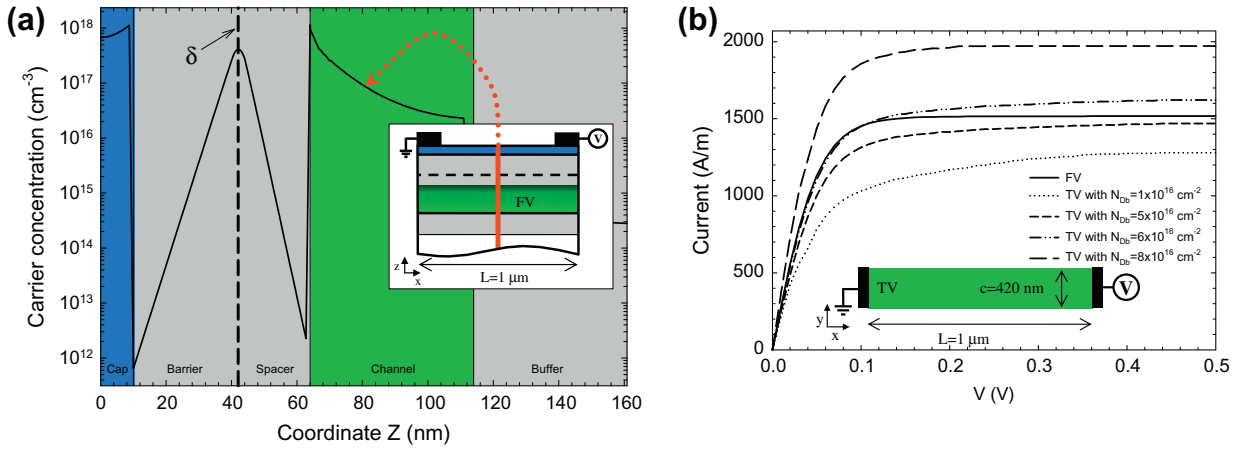

Fig. 9. (a) Front-view (FV) simulation in the plane *xz* using a structure of length, $L = 1$ μm. Third dimension *y* is homogeneous. A vertical electron concentration profile along the center of the FV in equilibrium condition ($V = 0$ V) for $\delta = 2 \times 10^{12}$ cm^{-2}. (b) TV simulations in the plane *xy* using structure where width is, $c = 420$ nm and $L = 1$ μm. Current density versus applied voltage for FV and TV simulations for different values of N_{Db}.

was modeled as a 4 nm layer doped at 5×10^{18} cm^{-3}. A vertical profile of the electron concentration simulated using HD simulations is shown in Fig. 9a. The length of the simulated structure is 1 μm which indicates the non-ballistic nature. It can be estimated from the figure that the channel population along the interface of spacer and channel is $n_s = 0.6 \times 10^{12}$ cm^{-2}. FV approach (*xz* plane) is useful for a homogeneous structure, but for a more complex structure like BDT where *y* dimension is not homogeneous, a TV simulation (in the *xy* plane) is valuable to account for the effect of third dimension. To explain this, TV simulations were done using different background doping (N_{Db}) [38] and *I–V* curves were obtained. The structure simulated is shown in inset of Fig. 9b. The length chosen is 1 μm which is same as FV simulations and a width is $c = 420$ nm because this will be the width of the channel of the BDT to be simulated later. To compare *I–V* curves obtained from TV with the FV, first we normalized with the width of the channel. Then, each TV current values were multiplied by a factor of n_s/N_{Db} using n_s from FV and the corresponding N_{Db}. From Fig. 9b the N_{Db} which gives best fit of TV with FV simulations is 6×10^{16} cm^{-3}. This background doping value was then chosen as the carrier concentration for further simulations of BDT where only the complicated top geometry of the InGaAs channel will be simulated.

The actual dimensions of the optimized fabricated device reported in the previous section have been implemented in the simulator. The carrier mobility of 11,000 cm^2/Vs and a saturation velocity of 6.7×10^7 cm/s for the 2DEG $In_{0.53}Ga_{0.47}As$ channel were employed. It is known that along the interface of InGaAs channel and the insulator (air), a depletion width of about $W_d \approx 40$ nm is associated, which reduces the effective channel width. To take this into account, a channel of 420 nm (=500−2 × 40 nm) is used for simulation purposes. At the interface of semiconductor and insulator, the Neumann boundary condition of

$$\hat{n}\varepsilon_1 \nabla_{\psi 1} - \hat{n}\varepsilon_2 \nabla_{\psi 2} = \sigma_S = 0 \tag{10}$$

is applied, where *n* is the unit normal vector, ε_1 and ε_2 are the permittivities of the materials on either side of the interface and σ_s is the sheet charge, which is zero at the interface in our case. Future simulations will include this effect through a negative density charge implemented as a Neumann boundary condition for the Poisson equation to fit the results more precisely. Ohmic contacts are implemented as simple Dirichlet boundary conditions, where surface potential and carrier concentration are fixed. Electrons quasi-Fermi potentials are equal to the applied bias of the electrode. The potential is fixed at a value that is consistent with space charge neutrality. It is to be noted that our devices are larger than the De-Broglie electron wave length, so quantum mechanical effects are not taken into account. Under these conditions, the considerable amount of thermal energy of the electrons (as compared with the quantized energy level steps) is enough to hide the quantum effects which may appear at low temperatures.

In the following study, our objectives are to investigate and understand the dependence of performance of BDT on the remaining geometrical parameters such as *t* and *c* through HD simulations. All simulations are performed for $V_{TD} = V_{RD} = V_{LD} = 1$ V, $V_{SS} = 0$ V at RT. For initial simulations the dimensions of the BDT with the geometry sketched in Fig. 4 are $b = h = 420$ nm, $k = 380$ nm and $a = 320$ nm.

4.1. Trench width optimization

In BDT, electrons are steered by the lateral electric field generated by gate sweep, which yields a possibility of BDT being worked below k_BT/e limit [43], offering low power consumption. Since the lateral electric field steers electrons in the channel because of its strong coupling, it attributes to the reduction of charge screening effects. Therefore, it becomes imperative to study the trench width, *t*, and its effects on the device performance for its optimization. Since experiments are for $t = 120$ nm and to account for the depletion of 40 nm along the trenches, for simulations, $t = 200$ nm (=120 + 40 × 2) is chosen. Consequently to study the trench width effect, other *t* values chosen are 160 nm and 120 nm which corresponds to $t = 80$ nm and 40 nm in actual device respectively. Keeping $b = h = 420$ nm, $s = 580$ nm and $c = 420$ nm, in Fig. 10a, the dependence of output and top drain leakage with *t* is shown. The output characteristic and top drain current reproduces qualitatively the main features of the experiments. Especially, the agreements in the maximum current values are quite satisfactory. Also, the current peak gate voltage (pinch-off) obtained in simulations is closer to the experiments. The changes and shapes in currents for I_{LD} and I_{TD} are consistent and in agreement with the experimental results as well. Fig. 10b shows that the concentration of electrons increase towards positive gate region and is maximum for $t = 200$ nm. It clearly indicates that the effect of increased trench width is an increase in the output current. A decrease in *t* for a specific voltage condition increases strong electric field (*x* component of electric field) along the trench, as can be seen in inset of Fig. 10b, resulting into increased steering effect, which reduces the peak output current due to early pinch-off. The profiles shown are

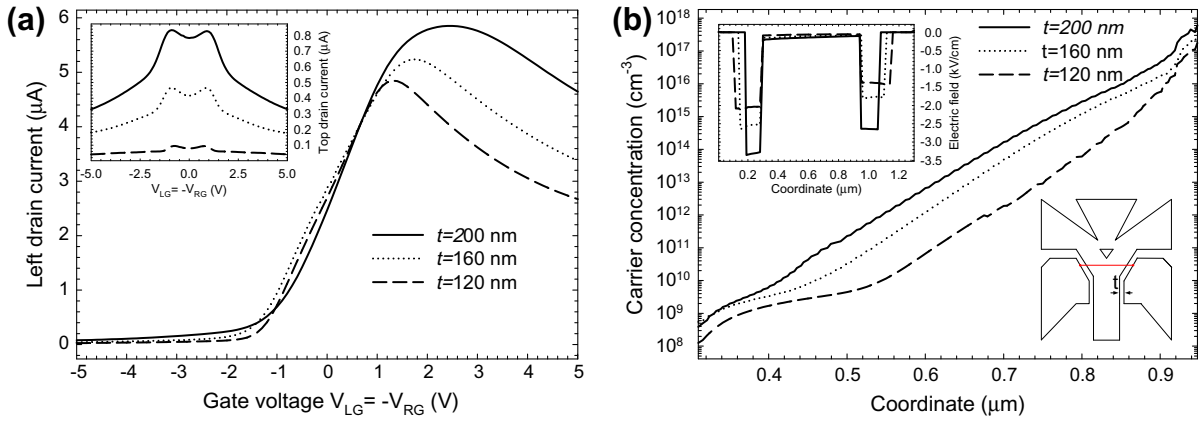

Fig. 10. (a) Left drain output and top drain leakage (in inset) for different trench widths t. (b) Electron concentration distribution and electric field (x component of electric field) profiles extracted at $V_{LG} = -V_{RG} = -2.5$, -1.7 and -1.3 V for $t = 200$, 160 and 120 nm respectively along the horizontal line shown in the schematic inset of BDT. Channel width $c = 420$ nm.

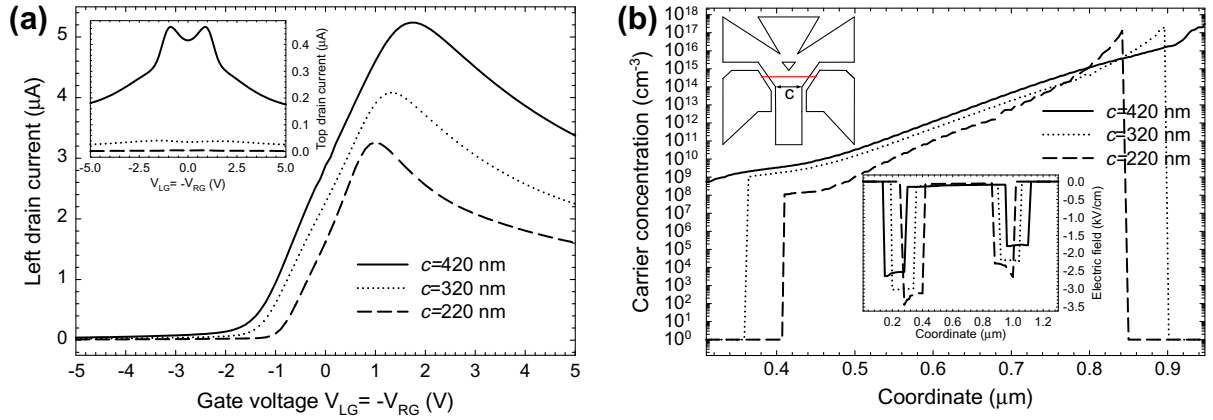

Fig. 11. (a) Left drain output and top drain leakage (in inset) for different channel width c. (b) Electron concentration distribution and electric field (x component of electric field) profiles extracted at $V_{LG} = -V_{RG} = -1.7$, -1.3 and -0.9 V for $c = 420$, 320 and 220 nm respectively along the horizontal line shown in the schematic inset of BDT. Trench width $t = 160$ nm.

extracted at $V_{LG} = -V_{RG} = -2.5$, -1.7 and -1.3 V (just at the maximum of the I_{LD}–V_{LG} characteristics) for $t = 200$, 160 and 120 nm respectively. A trade-off between lower pinch-off voltage and higher output current is employed, thereby choosing $t = 160$ nm for further simulations.

4.2. Channel width study

The purpose of this section is to simulate narrower channels to study the influence in the characteristic of this geometrical parameter. This type of study can be helpful in shrinking the device size in the future. For this purpose we have kept $s = 580$, 480 and 380 nm corresponding to $c = 420$, 320 and 220 nm respectively. Fig. 11a show the output and top drain leakage of the device for $c = 420$, 320 and 220 nm in which, as expected, the wider the channel, the more is the output current. Obviously the value of the current is directly related to the number of electrons inside the channel width. Also, the I_{TD} value is much smaller which indicates lesser leakage. In accordance with our experimental results [37], wider channels provide high current level, but the pinch-off is shifted to the higher gate bias. Asymmetry is enhanced for the narrower channels. To help in understanding the mechanism associated with the transport inside the device and also authenticate the obtained results in Fig. 11b, profiles of carrier concentration and electric field (x component of electric field) at $V_{LG} = -V_{RG} = -1.7$, -1.3 and -0.9 V (just at the maximum of the I_{LD}–V_{LG} characteristics) for $c = 420$, 320 and 220 nm respectively are plotted. The selected values provide the same applied electric field along the channel and allow for the comparison of the three channel widths. An increase in current with c can be understood from Fig. 11b where an increase in c increases the carrier concentration which results into higher current levels. High steering and decrease in the current are dependent on the pinch-off gate voltage which depends on the field in the channel.

With all above optimizations our proposed BDT device, with 500 nm channel width, for future fabrications and testing will have a specific geometry with $k = 420$ nm, $a = 400$ nm, $s = 665$ nm, $b = 500$ nm, $h = 500$ nm and $t = 80$ nm taken into account a depletion width of around 40 nm.

5. Conclusions

Room temperature properties of a nanoelectronic device, BDT, were studied. It was investigated experimentally that BDT shows nonlinear behavior due to its geometry and not due to its ballistic nature. The geometry of BDT was studied comprehensively to optimize its performance both using DC experimental measurements and ATLAS numerical simulations. BDTs with various dimensional parameters were fabricated and DC measured under different bias conditions for its optimum output and minimum leakage. The importance of deflector is examined and the position of deflector is optimized. The effect of change in bias conditions on the device

output is also inspected. In addition to experimental observations, by means of extended 2D hydrodynamic simulations, we optimized the performance of BDT by analyzing the effect of the remaining parameters. We performed simulations to determine background doping for 2D simulations to reproduce the real 3D effect. Trench width is optimized and it is found that decrease in trench width increases the channel-gate coupling. It is also verified that for narrower channels the gate control is more pronounced and pinch-off is obtained at a lower gate voltage.

Acknowledgments

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