INSTITUTE OF PHYSICS PUBLISHING SEMICONDUCTOR SCIENCE AND TECHNOLOGY

Semicond. Sci. Technol. **19** (2004) S199–S201 PII: S0268-1242(04)72228-2

2D ensemble Monte Carlo modelling of bulk and FD SOI MOSFETs: active layer thickness and noise performance

R Rengel, D Pardo and M J Martín-Martínez

Departamento de Física Aplicada, Universidad de Salamanca. Pza de la Merced s/n, 37008 Salamanca, Spain

E-mail: raulr@usal.es

Received 28 July 2003
Published 5 March 2004
Online at stacks.iop.org/SST/19/S199 (DOI: 10.1088/0268-1242/19/4/068)

Abstract

In this work, the RF and microwave noise performance of bulk and fully-depleted silicon-on-insulator (FD SOI) transistors with directly comparable topologies is investigated by means of an ensemble Monte Carlo simulator, and in the case of FD SOI devices, the influence of varying the active layer thickness is also studied. Intrinsic noise sources are calculated and analysed, and important figures of merit such as $NF_{\min}$ or R_n are also determined and evaluated. Moreover, a microscopic understanding of the noise phenomena is achieved, which is essential for the optimization of the transistors. FD SOI devices show a reduced influence of induced gate noise and drain noise as compared to the bulk transistor due to the minor influence of phonon scattering and energetic carriers at the pinch-off region. Whereas reducing the active layer thickness minimizes the effect of hot carriers in the noise parameters, it can lead to a degradation of other important high-frequency figures of merit such as g_m or f_T.

1. Introduction

Excellent high-frequency behaviour, together with a reduced influence of hot carriers and short-channel effects have been claimed for fully-depleted (FD) silicon-on-insulator (SOI) MOSFETs, thus becoming the mainstream alternative to bulk silicon MOSFET devices [1]. To profit from the advantages provided by FD SOI transistors, it is necessary to achieve a complete knowledge of their differences and similarities as compared to corresponding bulk devices operating in the RF and microwave frequencies range. In particular, the analysis of the noise performance of the transistors is critical in order to develop low-noise applications with a reduced cost. Nevertheless, the different geometrical and physical parameters of fabricated transistors make it almost impossible to perform experimental one-to-one comparisons between bulk and FD SOI MOSFETs [2]. Simulation tools are the best solution to carry out this study, thus helping to further develop silicon technologies.

In this work, we have employed a 2D ensemble Monte Carlo simulator (EMC) [3] to perform a complete investigation of the noise behaviour of 250 nm bulk and FD SOI n-MOSFETs with equivalent topologies (with the only exception of the presence of a buried oxide 400 nm thick in the FD SOI device, figure 1). Furthermore, in the case of the FD SOI transistor two different values for the active layer thickness (t_{si}), 30 nm and 50 nm, both corresponding to FD devices, were studied in order to evaluate the impact of this important parameter on the different figures of merit.

2. Static behaviour

The analysis of the inner quantities associated with charge transport is of great importance for the subsequent physical interpretation of the noise performance. Several magnitudes provided by the EMC simulator have been analysed: potential profiles, electric fields, velocity, energy and concentration of carriers, density of scattering mechanisms, etc. We found a very important influence of the buried oxide in the carrier transport conditions inside the channel: the FD SOI devices under study show a higher channel potential, a reduced density of phonon scattering mechanisms and lower electric fields

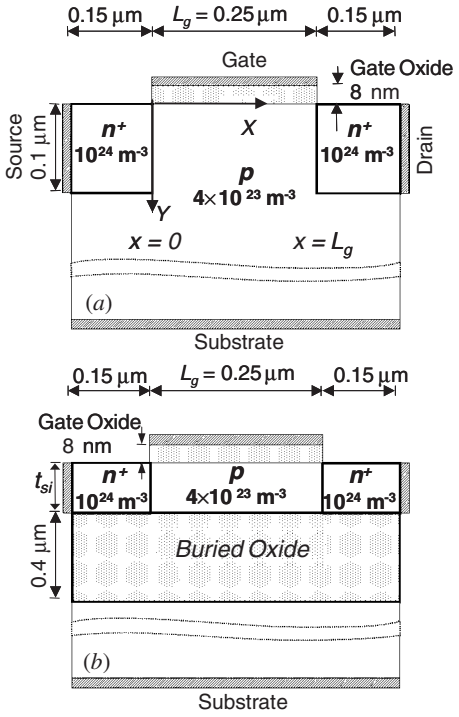

Figure 1. Scheme of the simulated devices: (*a*) bulk MOSFET and (*b*) FD SOI MOSFET.

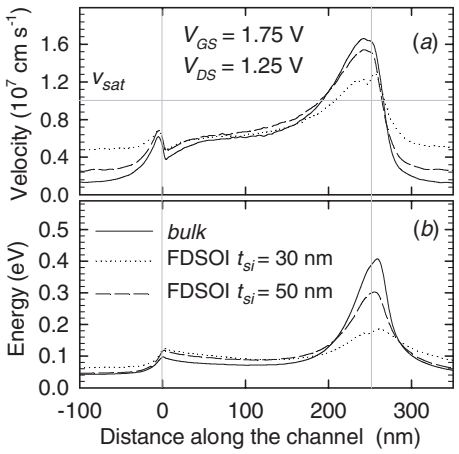

Figure 2. Velocity and energy of electrons along the channel in the three structures for $V_{GS} = 1.75$ V and $V_{DS} = 1.25$ V.

at the drain metallurgical junction and a thicker and more homogeneous inversion layer. As an example, in figure 2 we show the results for the energy and velocity of carriers along the channel for $V_{GS} = 1.75$ V and $V_{DS} = 1.25$ V for the three simulated structures. Results prove a reduced maximum energy and velocity overshoot for FD SOI devices at the pinch-off region as compared to the bulk transistor especially when the active layer thickness is reduced. This indicates a lower influence of hot carriers in the FD SOI MOSFETs under study than in the bulk device, with important consequences on the noise performance.

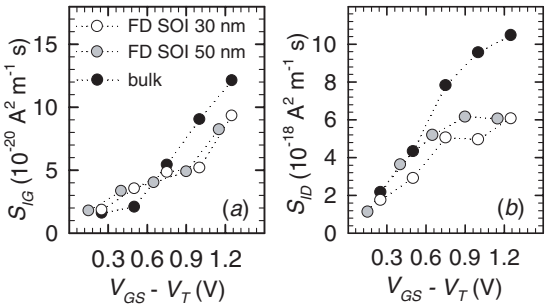

Figure 3. (*a*) S_{IG} and (*b*) S_{ID} as a function of $V_{GS} - V_T$ at 6 GHz for $V_{DS} = 1.25$ V.

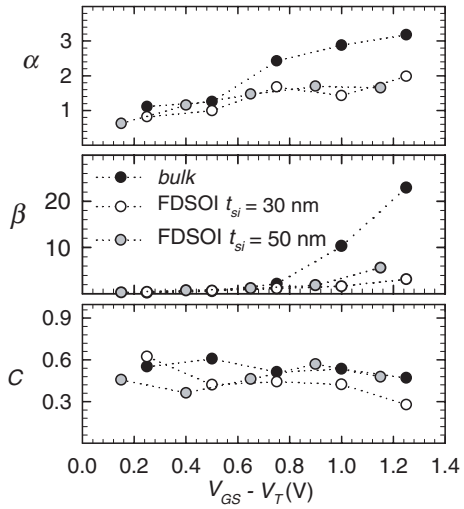

Figure 4. α, β and C parameters at 10 GHz as a function of $V_{GS} - V_T$ for the three structures, with $V_{DS} = 1.25$ V.

3. Noise performance

For the study of the high-frequency noise performance of the transistors, we considered a two-port device representation with two noise current generators: one at the output (drain)—associated with noise generated by carriers in the channel—and another at the input (gate)—related to noise induced by charge fluctuations under this terminal [4]. Both noise sources are correlated. The spectral densities of current fluctuations at terminals (S_{ID} at the drain and S_{IG} at the gate) are provided by the Monte Carlo simulator in a natural way, together with the cross-correlation (S_{IGID}), thus achieving a correct description of the noise behaviour. The frequency dependence of the spectral densities in the RF and microwave range has been found to be in excellent agreement with the general theory for FET devices [4]. With regard to the bias dependence, as an example figure 3 shows the results for S_{IG} and S_{ID} as a function of $V_{GS} - V_T$ for the simulated structures.

Nevertheless, in order to perform a straightforward comparison of the intrinsic noise in bulk and FD SOI devices, it is necessary to use the normalized noise parameters α, β and C [5], shown in figure 4. Those incorporate the spectral densities and the effect of dynamic parameters, which were calculated by means of the Fourier analysis of the transient response of terminal currents to voltage steps. In this way, it has been checked that a reduced coupling to the gate of

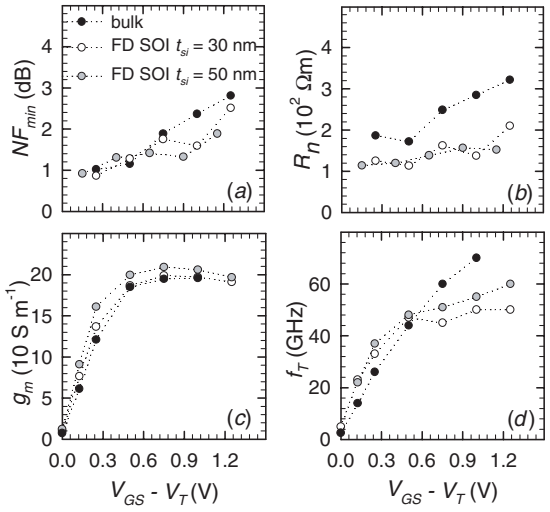

Figure 5. (*a*) $NF_{\min}$ at 10 GHz, (*b*) R_n at 10 GHz, (*c*) g_m and (*d*) f_T as a function of $V_{GS} - V_T$ for $V_{DS} = 1.25$ V in the three simulated structures.

charge fluctuations in the channel (lower β) exists for the FD SOI MOSFET, especially at high gate biasing. This effect is explained in terms of the more distributed charge transport in the active layer of the device induced by the presence of the buried oxide, which is also responsible for a thicker inversion layer, as observed in our EMC results. Moreover, an enhanced drain noise is obtained in the bulk transistor (larger α); this phenomenon is related to a reduced influence of scattering mechanisms at the drain in FD SOI transistors together with the lower peak energy obtained in this kind of device. The reduced effect of scattering mechanisms below the gate is also responsible for a minor correlation between both noise sources (C) in the FD SOI MOSFETs.

Finally, the typical four noise parameters employed in circuit analysis (minimum noise figure $NF_{\min}$, equivalent noise resistance R_n and phase and modulus of the complex optimum reflection coefficient Γ_{opt}) are also calculated [6]. As an example, we shall discuss the results concerning $NF_{\min}$ and R_n, which are usually considered as the main figures of merit of the noise generated by the device. In the case of $NF_{\min}$ (figure 5(*a*)) lower values are obtained in the FD SOI devices (especially for the device with $t_{si} = 50$ nm at high $V_{\text{GS}} - V_T$), mainly due to the reduced influence of both the noise generated in the channel and the induced gate noise. Nevertheless, it must be mentioned that at frequencies over the 20 to 30 GHz range, the bulk device presents enhanced values for this figure of merit as compared to the FD SOI transistors analysed. Regarding R_n, significantly lower values are observed in the FD SOI MOSFETs (figure 5(*b*)), in good agreement with the distributed nature of charge transport in the channel and the reduced influence of induced gate noise. This result indicates that using the FD SOI transistor it becomes easier to obtain the minimum noise condition in a low-noise amplifier design.

With regard to other important high-frequency figures of merit, in figure 5(*c*) and (*d*) we show the results for the intrinsic transconductance (g_m) and the cut-off frequency (f_T) as a function of $V_{GS} - V_T$. The FD SOI device with $t_{si} = 50$ nm offers the best results for g_m; in the case of the FD SOI with $t_{si} = 30$ nm, lower values are obtained, a fact that has been checked to be associated with the increase of channel access resistance due to the narrow active region, that becomes more prominent when the depth of the access regions is smaller than the maximum depletion region corresponding to the doping concentration of the substrate (55 nm in the devices under study). Regarding f_T, better values are obtained at high V_{GS} for the bulk device, whereas the FD SOI transistors offer poorer results as t_{si} is reduced. Our results indicate that this is due to the behaviour of the gate-to-source capacitance, which is progressively higher in the FD SOI MOSFETs as the active layer is thinner.

4. Conclusions

A detailed investigation of the high-frequency noise performance of 250 nm bulk and FD SOI transistors with directly comparable topologies has been performed by means of an ensemble Monte Carlo simulator. Results show that in the case of FD SOI transistors a significantly reduced influence of induced gate noise and drain noise is obtained, a fact that is associated with the lower carrier energies observed at the pinch-off region and the minor influence of phonon scattering mechanisms. Reducing the active layer thickness allows us to minimize the effect of hot carriers on the high-frequency noise; in contrast, the corresponding increase of access resistances leads to a fall off in the advantages provided by a narrower active region in terms of g_m and f_T.

Acknowledgments

This work has been funded by Research Project TIC2001-1754 from the Ministerio de Ciencia y Tecnología (and FEDER) and Research Project SA057/02 from the Consejería de Educación y Cultura de la Junta de Castilla y León.

References

[1] Cristoloveanu S 2001 *Solid-State Electron.* **45** 1403
[2] Colinge J P 1997 *Silicon-on-Insulator Technology: Materials to VLSI* 2nd edn (Norwell: Kluwer)
[3] Rengel R *et al* 2002 *Semicond. Sci. Technol.* **17** 1149
[4] van der Ziel A 1986 *Noise in Solid State Devices and Circuits* (New York: Wiley)
[5] Dambrine *et al* 1999 *IEEE Trans. Electron Devices* **46** 1733
[6] Greaves S D and Unwin R T 1993 *Microwave Opt. Tech. Lett.* **6** 60