Solid-State Electronics 193 (2022) 108289

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Monte Carlo analysis of thermal effects in the DC and AC performance of AlGaN/GaN HEMTs

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ARTICLE INFO

Keywords:
AlGaN/GaN HEMT
Monte Carlo
Thermal effects
Thermal resistance
Heat-conduction equation
Small-signal equivalent circuit

ABSTRACT

The influence of thermal effects in AlGaN/GaN HEMTs is studied by means of Monte Carlo simulations. Measured output and transfer characteristics of a transistor are well reproduced using two techniques, a thermal-resistance method and an electrothermal model which solves the steady-state heat-conduction equation. The validity of the model to reproduce the experimental results is checked in two-terminal structures and transistors. Both methods are also employed to investigate in AC regime in terms of the elements of the small-signal equivalent circuit, providing a good agreement with experimental values, with no significant differences between the models. Apart from the expected decrease of transconductance and drain conductance, the gate to source capacitance is also found to be lowered by heating effects.

1. Introduction

Gallium nitride (GaN) has become a semiconductor of great interest to develop high-power RF electronics required for applications like radar, electronic warfare, electric power generation and management, or mobile telecommunications [1]. Its high bandgap (~3.4 eV) and breakdown field (~3.3 MV/cm) make it an excellent material for working with high power and/or at high temperatures. Its high electron mobility (~2000 cm^2/Vs) and saturation electron velocity (~1.5×10^7 cm/s) make it also a competitive material for high–frequency applications [2]. As candidates to work under high voltages and currents, GaN-based devices usually show a remarkable heat generation [3,4]. Therefore, thermal effects due to self-heating are not a negligible problem [5,6]. Despite the influence of mechanisms like (non-radiative) recombination heat or convection, the power dissipation due to Joule effect is considered to be the main source of temperature increase in high-power semiconductor devices [7]. The temperature rise produced during their operation affects their reliability and lifetime, so that the characterization and mitigation of thermal effects is essential for industrial applications [8]. For this sake, models replicating the self-heating mechanisms are required. These mechanisms are accounted for by different methods (coupled to the electron-transport models) [9], like the thermal resistance method (TRM), the current density–electric field ($\vec{J} \cdot \vec{E}$) technique or the resolution of the heat conduction equation, called in this work electro-thermal model (ETM) [10–12].

High-electron-mobility transistors (HEMTs) were developed in the search of faster devices for high-frequency applications, and, in the case of GaN transistors, also for high-power applications. Apart from the DC behavior, the analysis of the AC performance of HEMTs is mandatory. Small-signal modeling approximates the (nonlinear) behavior of electronic devices at each bias point by means of linear equations, allowing to determine the so called Small-Signal Equivalent Circuit (SSEC) [13,14]. This type of analysis can be performed both from experimental and physical modeling points of view.

The aim of this work is to analyze self-heating effects in AlGaN/GaN HEMTs both in DC and AC regimes. To this end, the influence of thermal effects in two-terminal structures and transistors is studied by means of Monte Carlo (MC) simulations using two different thermal models, whose validity is confirmed by comparison with DC *I-V* curves and different elements of the SSEC determined experimentally.

With the ETM model, the precise location of the heat generated by phonon emissions allows to calculate a map of temperature inside the device and locate the position of the hotspots depending on the bias conditions. The non-uniform distribution of heat generation, and consequently of temperature, may have an influence on the AC operation of the devices, which here is analyzed by comparing the values of the different parameters of the equivalent circuit determined by means of the TRM (which assumes a uniform temperature) and the ETM.

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https://doi.org/10.1016/j.sse.2022.108289
Received 15 October 2021; Received in revised form 21 January 2022; Accepted 11 March 2022
Available online 12 March 2022

This paper is organized as follows. In "*Devices and tools*" section, the device under analysis and the tools used in the calculations are presented. In "*Result*" section, the results are organized in three subsections. The first one presents the calibration of the simulations in two-terminal structures (resistors). Next, the measured and simulated DC curves of the transistor at ambient temperature are discussed, demonstrating that the inclusion of the contact resistances in isothermal simulations is not enough to reproduce the measured curves and self-consistent electrothermal models are required. The last subsection corresponds to the study of the influence of thermal effects in the microwave domain. Finally, the main conclusions are given in "*Conclusions*" section.

2. Devices and tools

The HEMTs characterized in this work are based on an AlGaN/GaN heterojunction grown on a silicon substrate. The heterostructure is composed of a 14 nm thick AlGaN (29% Al) layer, on a 1.73 μm thick GaN buffer, with a 1 nm thick AlN spacer in the middle and a 0.5 nm thick GaN cap layer on the top. This heterolayer has sheet carrier concentration of $n_s = 1.3 \times 10^{13}$ cm^{-2}, Hall mobility of 1800 cm^2 V^{-1} s^{-1}, and average sheet resistance of 245 Ω_{sheet} at 300 K (after passivation with N_2O pretreatment and 150 nm of SiN). More details about the optimization of the heterolayer and the technological process for the fabrication of the transistors that have been used in this work can be found in [15,16]. In this paper, the experimental results and MC simulations correspond to a device with two gate fingers of 25 μm width, a gate length of 150 nm, a source-to-gate distance of 600 nm and a drain-to-source distance of 1.5 μm. Resistors for transfer length measurements (TLMs) of 4 lengths (2, 5, 10 and 20 μm) fabricated on the same wafer have also been measured.

The DC experimental results were obtained by means of a Keithley 4200-SCS semiconductor analyzer and the RF measurements with an Agilent PNA-X N5244A VNA, while the simulations were done with an in-house semi-classical electrothermal MC simulator using the two mentioned thermal models.

Fig. 1 shows a sketch of the simulated HEMT, including the values of the surface and polarization charges considered at the different interfaces. As shown in the figure, ohmic contacts are placed at the lateral sides of the devices, following the models presented in [17,18]. Details and parameters of the MC transport model can be found in [19,20]. In order to reproduce electron mobility in the channel, dislocation scattering and roughness scattering at the AlGaN/GaN heterointerface have been also considered [12].

Once MC simulations are performed, a post-processing of the obtained results must be done to compare with the experimental data, consisting in including the voltage drop at the source and drain ohmic contacts resistance R_C and the shift in V_{GS} associated to the Schottky contact V_{SCH}. Following the method explained in [21] (see the schematic picture of Fig. 1), the transformations needed to obtain the extrinsic drain-source and gate-source voltages (V_{DS} and V_{GS}) are.

$$V_{DS} = V_{DS}^{MC} + I_D^{MC} \times (2R_C + R_{sheet} \times l) \quad (1)$$

$$V_{GS} = V_{GS}^{MC} + V_{SCH} + I_D^{MC} \times (R_C + R_{sheet} \times l) \quad (2)$$

being V_{DS}^{MC} and V_{GS}^{MC} the intrinsic drain-source and gate-source voltages, respectively, used in the MC simulations. Note that we include an additional term $R_{sheet} \times l$, with R_{sheet} the sheet resistance of the heterolayer, which comes from the ohmic behavior of a small portion of the source-to-gate region of length l that is not considered in the simulation to save computation time ($l = 300$ nm, since the simulated L_{GS} is 300 nm while in the real HEMTs is 600 nm). This strategy reduces the time required by the simulations without losing accuracy in the results because of the ohmic nature of transport in such region.

Two models, TRM and ETM, are considered to analyze thermal effects. The first one employs a thermal resistance R_{TH} to calculate a bias dependent temperature which is uniform in the whole simulation domain. At each bias point (I_D^{MC}, V_{DS}^{MC}), the device is simulated at a constant temperature, T_{latt}, which is computed as.

$$T_{latt} = 300K + R_{TH} \times P_{Diss}, \quad (3)$$

with $P_{Diss} = I_D^{MC} \times V_{DS}^{MC}$ the intrinsic DC power.

The second approach consists in self-consistently coupling our electron-transport MC simulator with the solution of the steady-state heat conduction equation (HCE).

$$\nabla[\kappa(\vec{r})\nabla T(\vec{r})] = -G(\vec{r}), \quad (4)$$

where $T(\vec{r})$ and $G(\vec{r})$ are the local temperature and the dissipated power density, respectively, and $\kappa(\vec{r})$ the thermal conductivity (considered to be independent of temperature). It is to be noted that in both models all scattering probabilities, injection and Fermi distributions need to be self-consistently recalculated accordingly to the new temperature values (global or local) to run the subsequent MC iteration [12].

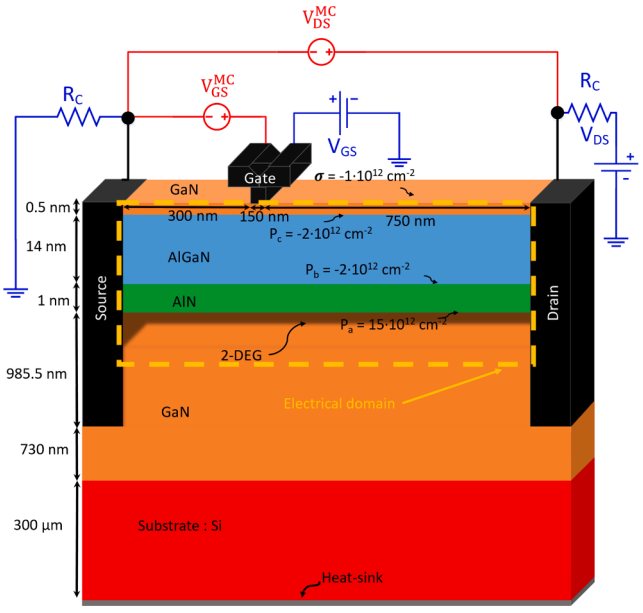

Fig. 1. Sketch of the simulated HEMT, together with the scheme for the inclusion of contact resistances in the HEMT. Blue lines stand for external or experimental elements and red ones for intrinsic MC values. The values used for the surface charges at the semiconductor-air interface, σ, and the AlN/GaN, AlGaN/AlN and GaN/AlGaN interfaces (P_a, P_b and P_c, respectively) are also indicated. The nominal value for the sheet electron density is $n_s = \sigma + P_a + P_b + P_c = 10^{13}$cm^{-2}, the one measured in the real epilayer. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

3. Results

3.1. Resistors (TLMs)

We have simulated the I-V curves of TLMs with lengths L of 0.5, 0.75, 1, 2 and 5 μm and measured TLMs with lengths of 2, 5, 10, 20 μm. Lengths longer than 5 μm require too long times to be simulated. The epilayer structure of the TLM is the same as the one shown for the HEMTs in Fig. 1, with the only difference that the gate is not present. In Fig. 2, we plot the comparison of the resistance R extracted from both simulated and experimental (the 4-wire, or Kelvin, method has been employed) results, jointly with the ideal dependence of R on L (including the influence of the contact resistances). The simulations well reproduce

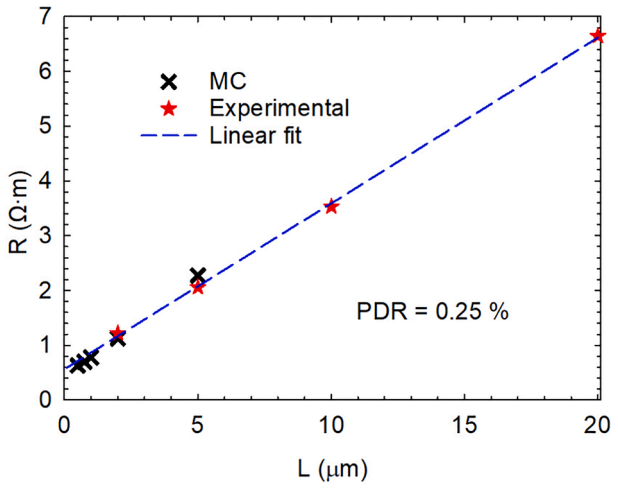

Fig. 2. *R* vs. TLM length comparing experimental and MC results for PDR = 0.25 %.

the measurements of the TLMs of the wafer for a percentage of diffusive reflections (PDR, associated to roughness scattering) at the GaN/AlGaN interface of 0.25%, indicating that the values chosen for the parameters of our model reasonably reproduce the carrier mobility in the heterostructure and the square resistance of the epilayer.

As first approximation, and in order to check the impact of thermal effects on the I-V curve, we compare the results of the TRM model and the experimental measurements at 300 K. In Fig. 3 we show *I-V* curves simulated using different values of R_{TH}. In the background, in color scale, the value of T_{latt} calculated with $R_{TH} = 20$ mm·K/W is represented to provide an idea of the temperatures reached inside the device at each bias point. As expected, the current obtained within the TRM is smaller than that calculated at a constant temperature of 300 K. While the agreement at low *V*, where dissipation is small, is still good, it is remarkable the improved current saturation obtained in simulations with the TRM at high voltages, which is now much more like that of experimental data. We can conclude that TRM modeling constitutes a significant advantage with respect to the isothermal study, where the current does not saturate. The simulations with the ETM do not provide an additional improvement, as the temperature is almost homogeneous in the whole structure (see the comparison made in [12] for a similar

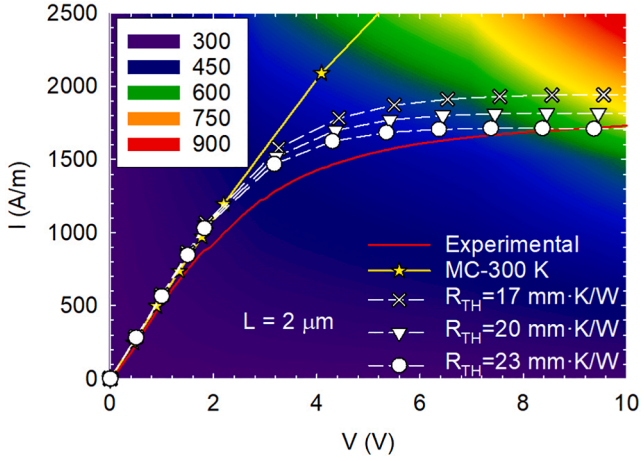

Fig. 3. Simulated *I-V* characteristics considering the TRM with different values of R_{TH} for the TLM with $L = 2$ μm, as compared with the experimental *I-V* curve measured at 300 K. The results of isothermal simulations at 300 K are also shown in order to evidence the effect of the self-heating. The background color represents T_{latt} obtained for $R_{TH} = 20$ mm·K/W.

TLM). Indeed, the *I-V* curves obtained with the ETM (with adequately chosen parameters, as will be explained later in Section 3.2) are not shown in Fig. 3 since they practically coincide with those of the TRM using $R_{TH} = 20$ mm·K/W. Finally, it is to be noted that for 10 V the predicted temperature is almost 700 K.

3.2. Transistors. DC behavior

In order to find the parameters which best fit the experimental data of the transistor under analysis ($L_G = 150$ nm, $L_{DS} = 1.5$ μm and $W =$ 2x25 μm), we have implemented the transformations of Eqs. (1) and (2) with different values of R_C and V_{SCH} and the experimental value of $R_{sheet} = 300\ \Omega_{sheet}$. The more suitable values to replicate the low-bias regime are $V_{SCH} = 4.5$ V and $R_C = 1\ \Omega$·mm, which we will use in next sections. Like in the case of TLMs, using a uniform simulation temperature of $T =$ 300 K, it is not possible to reproduce the experimental behavior under high current conditions, in particular the maximum drain current I_D^{MAX}. Self-heating effects must be taken into account to this end.

Within the TRM, we have done simulations with different values of R_{TH} in order to find the optimal one. Fig. 4(a) shows the simulated output characteristics of the transistor considering the optimum thermal resistance $R_{TH} = 19.25$ mm·K/W. It can be observed that the inclusion of

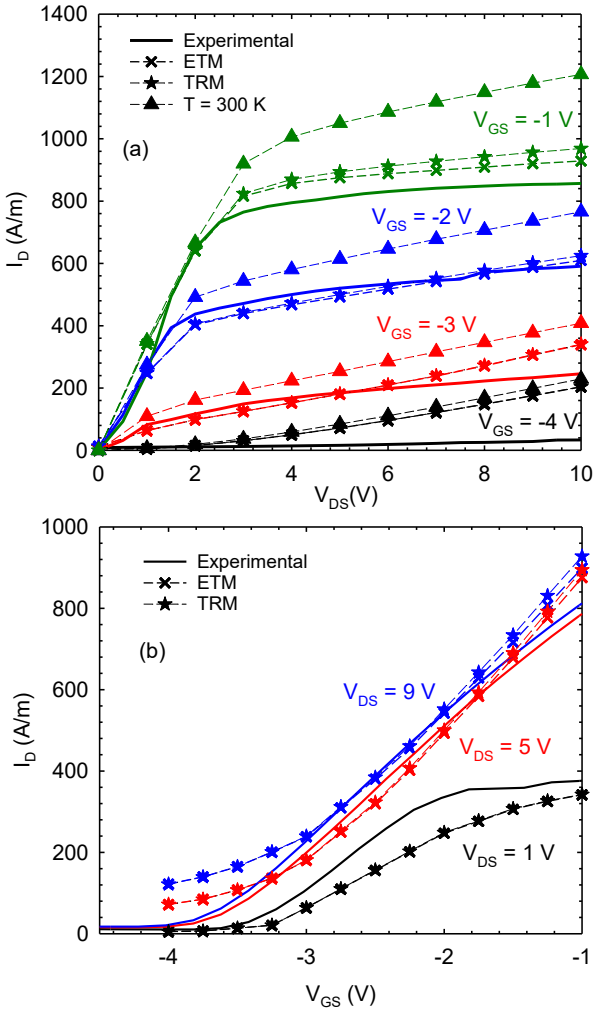

Fig. 4. (a) Output and (b) transfer characteristics obtained with the MC simulations including $R_C = 1\Omega$mm, and $V_{SCH} = 4.5$ V using thermal effects with the ETM (crosses) and TRM with $R_{TH} = 19.25$ mm·K/W (stars) and without considering thermal effects (triangles) as compared with measurements (lines) at $T = 300$ K.

thermal effects allows to correctly reproduce the levels of current. Even though the simulated current levels are still systematically higher than the experimental ones, for an intermediate value of V_{GS} simulations and measurements are in a reasonably good agreement. Using a higher value of R_{TH} would reduce the current in open channel conditions because of a much higher T_{latt}, but the low-power region would not be properly reproduced even much increasing the value of R_{TH} [22]. Near pinch-off conditions, the MC values of I_D are higher than the experimental ones, but not due to thermal effects in this case. The channel cannot be completely closed due to strong drain-induced-barrier-lowering effects (DIBL) taking place in the simulations [23]. These short-channel effects are typically mitigated in the fabrication of the devices with the inclusion of a p-type doping in the GaN buffer, as detailed in [24,25]. The p–type doping has the effect of a better confinement of electrons near the heterojunction, but it has not been included in the simulations since we decided to focus our work on the influence of thermal effects on the equivalent circuit of HEMTs for intermediate current levels, for which the agreement is already satisfactory.

The ETM simulation, thanks to the self-consistent solution of the HCE with MC electron transport, provides a non-uniform distribution of temperatures inside the device with local values in every mesh, which is closer to the actual physical conditions. To achieve a more realistic level of description of thermal effects, the thermal barrier resistance (TBR) between the GaN layer and the Si substrate has been taken into consideration with a value TBR $= 15 \times 10^{-8}$ m^{2}K/W [26]. This value has been chosen in order to obtain practically the same average temperatures than those of the TRM using the optimum $R_{TH} = 19.25$ mm·K/W (adequately reproducing the experimental results). Thus, the result is that the levels of current in ETM and TRM are very similar. On the other hand, in the transfer characteristics, plotted in Fig. 4(b), V_{TH} is also well reproduced at low V_{DS}, but DIBL effects are still the main reason of the disagreement with measurements, mainly for high V_{DS}. In any case, the curves obtained in the simulations for V_{GS} between −3.0 V and −1.0 V are in a reasonable agreement with the measurements and its levels of current.

In order to show the advantages provided by the ETM, in Fig. 5 we compare the temperature distributions obtained for the bias point $V_{DS} =$ 9 V, $V_{GS} = -3$ V, near pinch-off, with another one with a much higher gate voltage, $V_{DS} = 3$ V, $V_{GS} = -0.5$ V. The dissipated power is the same in both bias conditions, $P_{Diss} = 2.8$ W/mm. Fig. 5 shows that although the hotspot is different, slightly hotter, 364 K, in quasi pinch-off as compared to 358 K in open bias condition, the average temperature T_{av} = 350 K is similar in both cases. It is also interesting to observe the temperature profile along the channel, Fig. 5(c), showing that the position of the hotspot is in both cases in the gate-to-drain region. However, in quasi pinch-off conditions the temperature increase is highly focused at the drain side of the gate, while in open channel conditions it is more homogeneously distributed [10,27]. This makes that the temperature below the gate is appreciably higher near pinch-off, while it is in the gate drain-region where it is slightly higher when the channel is open.

3.3. Small-signal equivalent circuit

The objective of this section is to analyze the influence of self–heating and the associated temperature distribution under different bias conditions on the AC performance of the transistor, particularly, on the values of the capacitances of the SSEC. The SSEC of the HEMT is determined by means of MC simulations and compared with the values obtained experimentally from the S-parameters [21,28].

In order to obtain the AC parameters, we first simulate the device with the chosen DC values as initial condition for the subsequent current transients. Then, two transient simulations are performed, one with a voltage step applied at the gate ($\Delta V_{GS} = 0.05$ V) and another with a voltage step at the drain ($\Delta V_{DS} = 0.25$ V). These voltage steps are small enough to assume linear response (avoid harmonic generation) and high

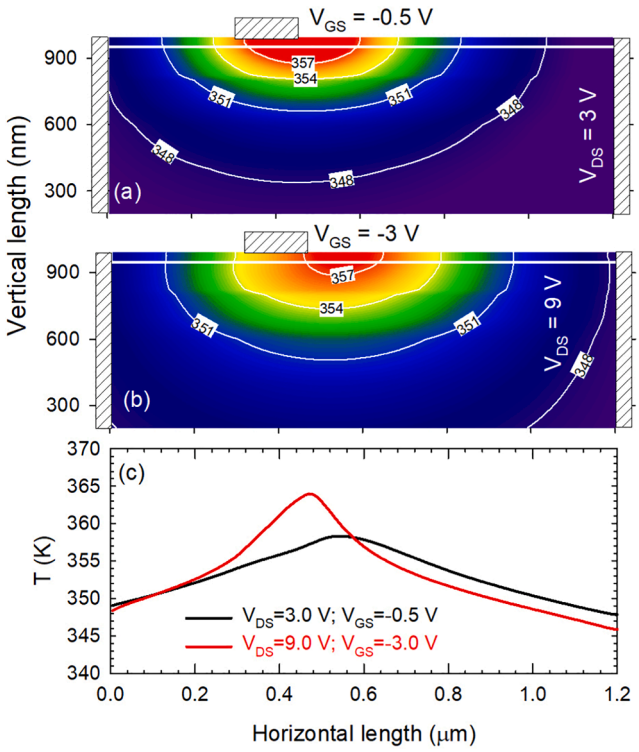

Fig. 5. Map of temperatures obtained in the electrical domain for the bias points: (a) $V_{DS} = 3$ V, $V_{GS} = -0.5$ V and (b) $V_{DS} = 9$ V, $V_{GS} = -3$V. Shaded areas indicate the positions of the contacts (the position of the channel is indicated by the white line). In (c) the temperature profiles at the channel for both bias conditions are shown.

enough to originate a significant change in the current level. To remove the stochastic noise, an average over 50 transients is performed. The temperature conditions in the simulation during the transient are considered to be those corresponding to the initial bias point.

The *Y*-parameters are then obtained from the Fourier Transform of the current transients and the parameters of the SSEC are finally computed using the standard FET configuration [29]. The consistency of the procedure and the validity of the SSEC model to describe the AC behavior of the transistor is confirmed by the fact that the different elements are found to be frequency independent up to more than 100 GHz. The effect of part of the extrinsic capacitive effects associated with the topology of the devices which cannot be de-embedded in the experiments has been added to the intrinsic SSEC as explained in [30].

In order to check the dependence of the SSEC elements on the biasing, we perform MC simulations at $V_{DS}^{MC} = 6$ V and different V_{GS}^{MC}. The results obtained for the SSEC capacitances with and without including heating effects are shown in Fig. 6 compared with the experimental values measured at $V_{DS} = 6$ V. The values of g_m and g_d are not presented because of the discrepancies with the experimental results already observed in the *I-V* curves of Fig. 4 (and also because they do not provide much new information).

In the previous section, we found that the ETM and the TRM provide similar current–voltage characteristics in DC regime, without a significant impact of the location of hotspots on the drain current, at least at DC level [12]. However, in the case of AC regime, since some of the SSEC parameters depend on the local carrier concentration (and energy distribution) and transport properties in some specific regions of the device, it is possible that differences arise between the TRM and the ETM values when heating is significant, since, while in the former the temperature is homogeneous in the device, in the latter it is position-dependent [10,31,32].

Fig. 6 shows that MC results well reproduce the measurements of C_{GD}

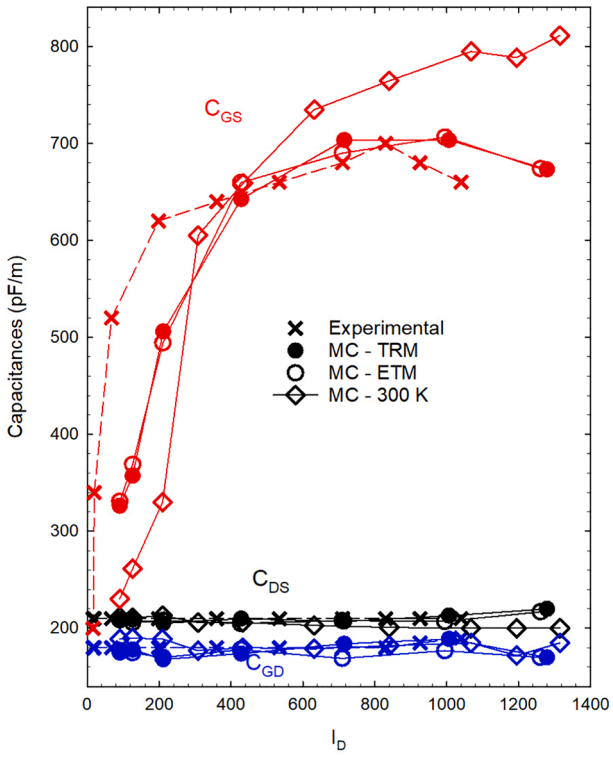

Fig. 6. Capacitances of the SSEC vs. I_D^{MC} for $V_{DS}^{MC} = 6$ V calculated with MC simulations at 300 K and including heating effects with both ETM and TRM. The experimental results obtained at $V_{DS} = 6$ V are also shown.

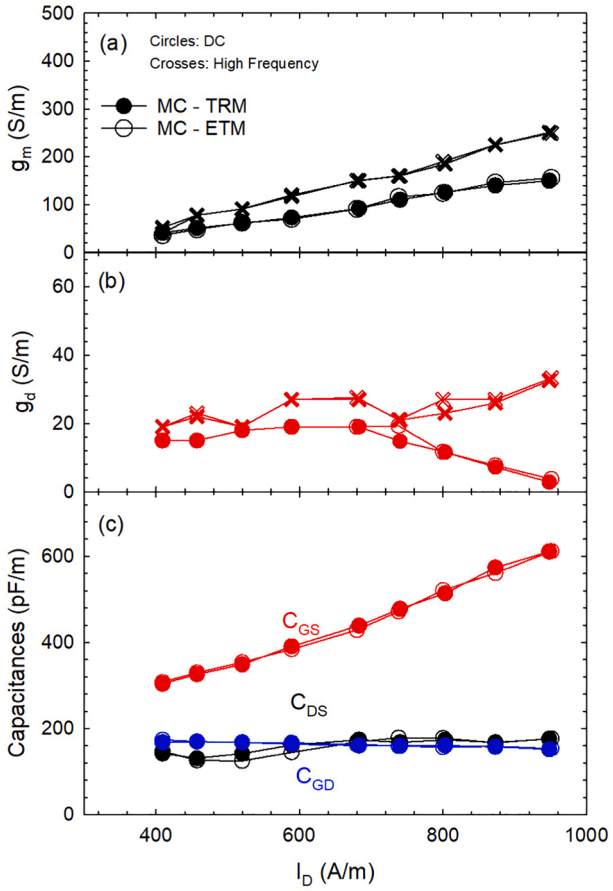

Fig. 7. SSEC elements obtained from MC simulations using ETM and TRM vs. I_D^{MC} for $V_{DS}^{MC} = 30V$: (a) transconductance, g_m, (b) drain conductance, g_d, and (c) C_{GS}, C_{GD} and C_{DS} capacitances. In (a) and (b) the values of g_m and g_d obtained from the static *I-V* curves (DC) and the transient simulations (high frequency) are shown.

and C_{DS}, whose values are nearly constant and independent of whether heating effects are considered or not in the simulations. In the case of C_{GS}, it is necessary to include the heating effects in the MC simulations in order to match the experimental results (with just a small discrepancy due to the shift in the values of I_D, already observed in the DC results of Fig. 4). On the other hand, the MC simulations at 300 K clearly overestimate the values of C_{GS} in open channel conditions, thus demonstrating that self-heating effects are of importance when performing the AC modelling of the transistors.

Another important result of Fig. 6 is that the ETM and TRM simulations provide practically the same result, thus confirming that non-uniform temperature distributions inside the transistor, as those shown in Fig. 5, have practically no influence on the values of the SSEC capacitances. This may be due to the fact that the level of dissipated power is not sufficiently high for $V_{DS}^{MC} = 6$ V. That is why we have performed simulations at bias points with much more dissipated power, increasing V_{DS}^{MC} to 30 V, for which a much higher hotspot temperature with respect to the average is expected to have a stronger impact on the values of the SSEC parameters and originate differences between those calculated with the TRM and the ETM.

Fig. 7(a) and (b) show the results of g_m and g_d obtained from the static *I-V* curves (thus considering the temperature variations between the different bias points) and the transient simulations (where the temperature is kept constant at that of the initial point, since we assume that the heating process is much slower than the current variations). Those limit values would correspond to the measurements performed at very low and high frequency, respectively, where the device temperature can follow or not the input signal. As expected, important differences are found between both results due to the strong heating effects arising at such high drain bias, which reduce the drain current and therefore the values of both g_m and g_d, the latter even taking negative values when the dissipated power increases.

The SSEC capacitances, plotted in Fig. 7(c), also show no significant differences between the outcome of ETM and TRM. Some variation in C_{GD} was expected due to the presence of the hotspot at the drain side of the gate, which could have an effect on the electron concentration distribution. However, within the precision of our simulations, no differences can be identified [33].

4. Conclusions

In this contribution, a MC device simulator coupled with thermal algorithms has been calibrated to reproduce the DC and AC experimental measurements of AlGaN/GaN HEMTs. First, the parameters of the MC simulation have been adjusted through isothermal simulations by comparison with the experimental resistance values for TLMs with different lengths. Simulations at different ambient temperatures evidence strong heating effects in the measured TLMs.

Once the simulator has been calibrated, the experimental output and transfer characteristics of a transistor with $L_G = 150$ nm have been replicated. To his end, we have included the effect of the contact resistances and the Schottky barrier. However, isothermal simulations are not capable of correctly reproduce the measured current when the dissipated power increases and self-heating comes into play. Two different electrothermal models have been considered: the TRM (based on a constant thermal resistance, with a value of $R_{TH} = 19.25$ mm·K/W) and the ETM (which accounts for local temperature variations by means of the solution of the HCE). MC simulations are also employed to extract the elements of the SSEC. MC simulations are also able to correctly reproduce the experimental results of the SSEC elements. However, as general conclusion, we do not find significant differences between the

results obtained with both thermal models, both allowing to achieve a much better agreement with the experimental DC and AC measurements than isothermal simulations. It is remarkable that, apart from the expected variations of g_m and g_d (given by the decrease of the drain current due to the self-heating), C_{GD} and C_{DS} are not much affected by heating. However, C_{GS} significantly decreases due to heating effects, both ETM and TRM simulations being able to correctly reproduce the experimental values.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

The authors would like to thank V. Hoel and Y. Cordier for providing the devices taken as reference to perform the simulations of this work.

This work has been partially supported through grant PID2020-115842RB-I00 funded by MCIN/AEI/ 10.13039/501100011033 and Junta de Castilla y León and FEDER through project SA254P18. H. Sánchez-Martín acknowledges his contract to the Junta de Castilla y León.

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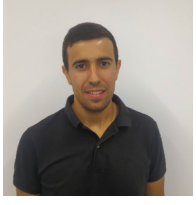

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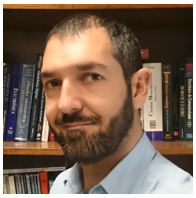

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