

Analysis of voltage noise in forward-biased silicon bipolar homojunctions: Low- and high-injection regimes

M. J. Martín,^{a)} D. Pardo, and J. E. Velázquez

Departamento de Física Aplicada, Facultad de Ciencias, Universidad de Salamanca, 37008 Salamanca, Spain

(Received 29 August 1997; accepted for publication 4 October 1997)

An ensemble Monte Carlo (EMC) simulator has been used to study bipolar transport in silicon p^+n and pn^+ homojunctions under forward-bias conditions, both in low- and high-injection regimes. The study focuses on a microscopic analysis of voltage fluctuations in such devices. The method of voltage-noise operation mode provides spatial analysis of the spectral density of voltage fluctuations under constant-current conditions. In the low-frequency range, the presence of shot, thermal, and excess noise due to hot carriers was found when the bias conditions were modified. Also, the EMC method permits ready evaluation of the noise equivalent temperature in both structures from the observed voltage fluctuations. © 1997 American Institute of Physics. [S0003-6951(97)01149-2]

Until quite recently, the development of high-speed devices has focused on unipolar III–V technologies. However, the recent development of a bipolar technology, such as that based on the Si–Ge (Refs. 1 and 2) alloy, has allowed the manufacture of high-performance heterojunction bipolar transistors (HBTs). Furthermore, the tendency to down scale the dimensions of devices has emphasized the importance of both a better understanding of far-from-equilibrium phenomena and a detailed characterization of electronic noise, which are relevant for optimizing the performances of bipolar devices. Accordingly, a good modeling of these phenomena begins with knowledge of the fluctuations in the microscopic processes of transport that cause noise (both in low and high frequencies). Before addressing the study of these more complex heterojunction devices, it seems appropriate to analyze the bipolar homojunction devices in which the transport properties associated with both types of carriers and their interaction must appear. Study of this can be carried out by means of an ensemble Monte Carlo simulation self-consistently coupled with a Poisson solver algorithm, which has previously and successfully been employed to investigate the fluctuations in different high-speed unipolar devices: n^+nn^+ junctions, Schottky diodes, and GaAs metal–semiconductor field-effect transistor (MESFET).^{3–6}

The simulated structures are modeled as abrupt Si $pn^+y p^+n$ junctions.⁷ The doping level of the $n^+y p^+$ regions is 10^{17} cm^{-3} , and such regions are $0.3 \mu\text{m}$ long, whereas the n and p regions doping density is $5 \times 10^{15} \text{ cm}^{-3}$, and these regions are $0.4 \mu\text{m}$ long. According to the doping densities, the built-in potential (V_{bi} is 0.735 V (300 K)). The microscopic model implemented in the simulator enables one to follow electron and hole dynamics simultaneously. The band structure considered includes the X and the L valleys of the conduction-band anisotropically.⁷ The valence-band model includes two nonparabolic bands (heavy and light) degenerated at the Γ point with spherical energy surfaces.⁷ Calculation of the physical quantities of interest is carried out following the standard scheme.⁸ Generation–recombination phenomena (band-to-band, band-

to-center,...) were not considered, owing to the small length of the devices.⁹ The device is divided into equal cells of 10 nm each; these are sufficiently small to reproduce the spatial variations in the electric potential. The time step to solve the Poisson equation is 10 fs .

The theoretical analysis to perform the study of the voltage fluctuations has been previously used in different unipolar devices.⁶ The theory underlying the method is based on the expression for the total current, $I(t)$. For a one-dimensional structure of total length L , that current is given by

$$I(t) = I_c(t) - \frac{A\epsilon_0\epsilon_r}{L} \frac{d}{dt} \Delta V(L, t), \quad (1)$$

where ϵ_0 is the free-space permittivity, ϵ_r the relative static dielectric constant of the material, A the cross-sectional area, $\Delta V(L, t)$ the instantaneous voltage drop between the terminals, and $I_c(t)$ the conduction current, which for a bipolar device can be written as

$$I_c(t) = \frac{q}{L} \sum_{i=1}^{N_{Te}(t)} v_i(t) - \frac{q}{L} \sum_{j=1}^{N_{Th}(t)} v_j(t), \quad (2)$$

where q is the absolute value of the electron charge, $v_i(t)$ and $v_j(t)$ are the instantaneous velocities along the electric-field direction of the i th electron or the j th hole, and $N_{Te}(t)$ and $N_{Th}(t)$ total number of electrons or holes, respectively, inside the device.

In order to analyze the voltage fluctuations inside the device (voltage-noise operation mode), the condition to be imposed is to keep the total current through the structure constant in time, i.e., $I(t) = I_0$. In these operation conditions, from Eq. (1) we obtain

$$\frac{d}{dt} \Delta V(L, t) = \frac{L}{A\epsilon_0\epsilon_r} [I_c(t) - I_0]. \quad (3)$$

In each time step, Δt , this relationship gives the instantaneous voltage drop between the terminals:⁵ the deviation of $I_c(t)$ from I_0 yields us $\Delta V(L, \Delta t)$. With a sufficient number of time steps and through the resolution of the Poisson equation, this procedure allows one to calculate the instantaneous voltage fluctuations along the device: $V(x, t = n\Delta t)$. Conse-

^{a)}Electronic mail: mjesus@rs6000.usal.es

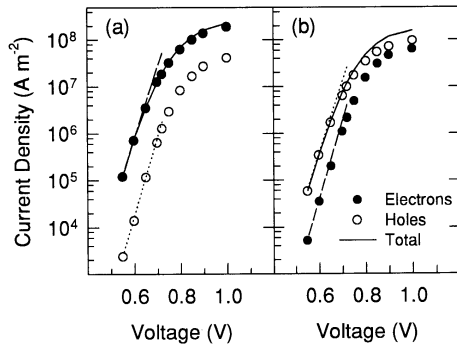


FIG. 1. Total current density (continuous line), electron current (closed symbols), and hole current (open symbols) as a function of average bias: (a) for the pn^+ structure and (b) for the p^+n structure. Also shown are the fits of the current density of electrons and holes by the theoretical equation of a short diode: discontinuous and dotted lines, respectively.

quently, this method provides the autocorrelation function and the spectral density of voltage fluctuations, respectively, $C_v(x, t)$ and $S_v(x, f)$, under constant total-current conditions, as a function of different positions inside the device as measured from one of the contacts.

Figure 1 shows the total forward density current (J)–voltage (V) characteristics of the (a) p^+n and (b) pn^+ structures (Fig. 1) for V close to V_{bi} . The electron and hole density currents are also plotted. When $V < V_{bi}$, the whole of the potential drop is essentially localized in the spatial charge region of the junctions (barrier-limited current transport). In this bias range, the simulation results show that the current in both structures exhibits exponential behavior, in agreement with the theoretical equation of a short diode.¹⁰ In both structures, for applied voltages above V_{bi} (high-injection regime), the junction barrier almost disappears and the voltage drops along the whole device. As a consequence, there is an electric field different from zero in the quasineutral regions. Under these conditions, the junctions behave as a “resistance” varying with the bias.

Figure 2 shows the spectral density of the voltage fluctuations, $S_v(x, f)$, (taking as a reference the contact in the n -type region in both structures) for a value of the average bias equal to 0.65 V. This value corresponds, respectively, to a total current density (I_0/A) equal to 3.57×10^7 and 1.94×10^6 A m⁻² in the pn^+ and p^+n structures. The effect of the plasma oscillations dominates the voltage fluctuations in the highly doped regions of both structures and, therefore, $S_v(x, f)$ exhibits a maximum at very high frequencies created by spatial growth into the highly doped region of each diode, which does not depend on the applied voltage. That maximum appears for a frequency value related to the majority carrier plasma frequency and the dielectric relaxation time of the n^+ and p^+ regions, respectively, for pn^+ and p^+n diodes. For the structures considered, the frequencies of $S_v(x, f)$ maxima are very different (around 1300 GHz in the pn^+ diode and close to 700 GHz in the p^+n one). This means that only the pn^+ have a well-defined maximum, whereas in the p^+n diode is masked by the contributions of the lower frequencies (thermal noise).

In contrast to the results of high frequencies, the behavior of the spectral density at low frequency is strongly de-

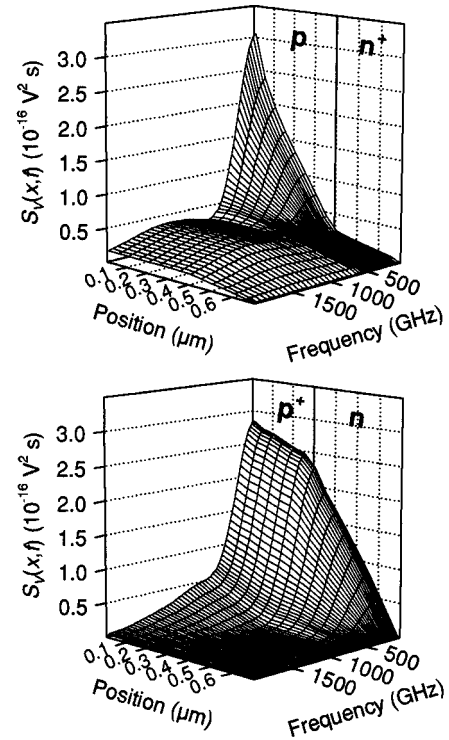


FIG. 2. Spectral density of voltage fluctuations as a function of frequency and position in the pn^+ structure (upper) and p^+n structure (down) for an average voltage equal to 0.65 V.

pendent upon the average voltage. The low-frequency value of the spectral density of the voltage fluctuations, $S_v(0, 0)$, is affected by different internal mechanisms that control the noise in the device and varies with the voltage (the presence of a barrier, velocity fluctuations in Ohmic conditions, hot carriers, etc.). This means that $S_v(x, 0)$ allows one to locate the positions of the different noise sources inside the structures. In view of these special characteristics, this quantity merits closer examination. In Fig. 3 we show $S_v(x, 0)$ for different average voltages in both structures. In the highly doped regions of both structures, resistance is essentially determined by the majority free-carrier concentration (equal to the doping density along the whole region). As a consequence of the large doping difference between both regions

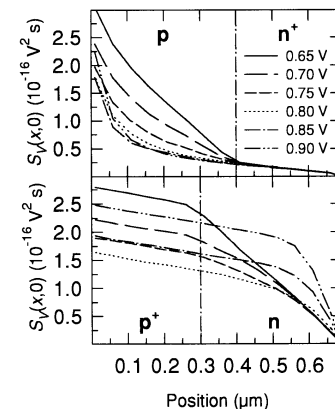


FIG. 3. Low-frequency value of the spectral density of voltage fluctuations, $S_v(x, 0)$, around different average voltages for both the pn^+ (upper) and p^+n (down) diodes.

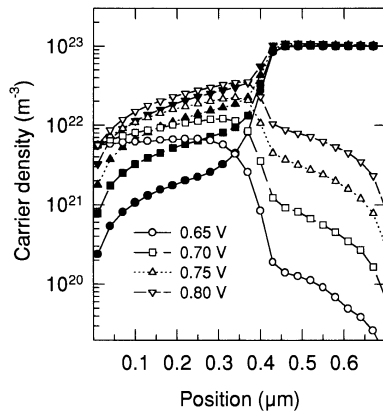


FIG. 4. Density of electrons (closed symbols) and holes (open symbols) in the pn^+ structure for different average voltages.

of the structures, in the n^+ and p^+ regions the carriers remain essentially close to the thermal equilibrium. Then, $S_v(x,0)$ exhibits a quasilinear increment with the position with no dependence on the average voltage, in accordance with the local value of the conductivity (the voltage fluctuations are measured from the n -type terminal). Furthermore, it can be seen that in the weakly doped regions of both structures $S_v(x,0)$ grows in a different way depending on the average voltage. Let us begin by trying to understand this dependence thoroughly; for this, we must consider different ranges of behavior.

For the lowest average-voltage considered (0.65 V), as a consequence of the barrier, the presence of the minority carriers in the lowly doped regions is weak. Nevertheless, with the increase in the average bias (in the 0.65–0.80 V range) in these regions, the minority carrier concentration increases and becomes non-negligible in relation to the majority carrier concentration. In this way, the resistivity of these regions decreases with the average applied voltage. This effect is strongly nonlinear with position, in consonance with the minority carrier profile (Fig. 4) and more pronounced in the pn^+ diode owing to the greater mobility of the electrons. This behavior of the low-doping regions resistivity agrees with that of the $S_v(x,0)$: when the average bias increases, the local resistivity decreases strongly near the metallurgical junction [which explains the lower slope of $S_v(x,0)$], and only maintains a high value in a gradually thinner zone close to the terminal in the weakly doped regions. Globally, in this bias range $S_v(0,0)$ decreases.

For average voltages above 0.80 V, the low-doping regions in both diodes are in a high-injection regime. There is an important accumulation of minority carriers, and the depletion region disappears. Owing to the quasineutral nature of these regions, the majority carrier profile follows that of the minority carriers. This effect establishes an electric field that increases with bias (particularly in a zone close to the terminal) and is responsible for a local heating of the carriers. This heating leads to transport degradation through a reduction in differential mobility. As a consequence of this, in the afore-mentioned zone close to the terminal in the weakly doped regions, a strong reduction in the conductivity appears, leading to a sharp rise in $S_v(x,0)$ for the high values of the bias plotted in Fig. 3 (from 0.80 to 0.90 V). Globally,

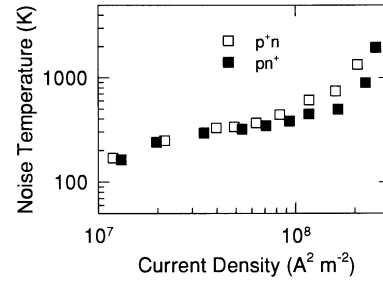


FIG. 5. Equivalent noise temperature at low frequency as a function of the total density current in the pn^+ (closed symbols) and p^+n (open symbols) structures for the voltage-noise operation mode.

in this bias range $S_v(0,0)$ increases with the applied bias.⁷

With a noise temperature study, we can confirm the great importance of the presence of hot carriers. Figure 5 shows the noise equivalent temperature at low frequencies³ as a function of the current density of both structures calculated through the voltage-noise mode operation. In both the low current and low bias ranges, noise temperature tends towards a value close to one-half of the lattice temperature. This agrees with a barrier-limited current regime and points to full shot noise behavior.^{11,12} As both current and average bias increase, thermal noise becomes important and noise temperature increases towards the lattice temperature. Nevertheless, for the highest currents (high-injection regime), the noise temperature surpasses the lattice temperature, in agreement with excess noise behavior due to the hot carrier effect commented on above (minority carriers of the low-doping regions in both structures). This shows that the sources of the excess noise are spatially located close to the terminal in the weakly doped regions.

This work was funded through Research Project No. TIC95-0652 from the CICYT.

¹J. N. Burghartz, K. A. Jenkins, D. A. Grützacher, T. O. Sedgwick, and C. L. Stanis, *IEEE Electron Device Lett.* **EDL-15**, 360 (1994).

²J. D. Cressler, E. F. Crabbé, J. H. Comfort, J. Y.-C. Sun, and J. M. Stork, *IEEE Electron Device Lett.* **EDL-15**, 472 (1994).

³J. Zimmermann and E. Constant, *Solid-State Electron.* **23**, 915 (1980).

⁴L. Varani, T. Kuhn, L. Reggiani, and Y. Perlès, *Solid-State Electron.* **36**, 251 (1993).

⁵T. González, D. Pardo, L. Varani, and L. Reggiani, *Appl. Phys. Lett.* **63**, 3040 (1993).

⁶T. González, D. Pardo, L. Varani, and L. Reggiani, *IEEE Trans. Electron Devices* **ED-42**, 991 (1995).

⁷M. J. Martín, D. Pardo, and J. E. Velázquez, *J. Appl. Phys.* **79**, 6975 (1996).

⁸C. Jacoboni and P. Lugli, *The Monte Carlo Method for Semiconductor Device Simulation* (Springer, Vienna, 1989).

⁹J. C. Manifacier, R. Ardebili, and C. Popescu, *J. Appl. Phys.* **80**, 2838 (1996).

¹⁰S. Tiwari, *Compound Semiconductor Device Physics* (Academic, New York, 1992).

¹¹A. Van der Ziel, *Noise in Solid State Devices and Circuits* (Wiley, New York, 1986).

¹²M. Trippe, G. Bosman, and A. Van de Ziel, *IEEE Trans. Microwave Theory Tech.* **MTT-34**, 1183 (1986).