Semicond. Sci. Technol. **14** (1999) 864–870. Printed in the UK PII: S0268-1242(99)03101-6

Effect of the T-gate on the performance of recessed HEMTs. A Monte Carlo analysis

Javier Mateos†, Tomás González†, Daniel Pardo†, Virginie Hoel‡ and Alain Cappy‡

† Departamento de Física Aplicada, Universidad de Salamanca, Plaza de la Merced s/n, 37008 Salamanca, Spain
‡ Institut d'Electronique et Microélectronique du Nord UMR CNRS No 9929, Département Hyperfréquences et Semiconducteurs, BP 69, 59652 Villeneuve D'Ascq Cédex, France

Received 30 March 1999, accepted for publication 17 June 1999

Abstract. A microscopic study of 0.1 μm recessed gate δ-doped AlInAs/GaInAs HEMTs has been performed by using a semiclassical Monte Carlo device simulation. The geometry and layer structure of the simulated HEMT is completely realistic, including recessed gate and δ-doping configuration. The usual T-gate technology is used to improve the device characteristics by reducing the gate resistance. For first time we take into account in the Monte Carlo simulations the effect of the T-gate and the dielectric used to passivate the device surface, which affects considerably the electric field distribution inside the device. The measured I_d–V_{ds} characteristics of a real device are favourably compared with the simulation results. When comparing the complete simulation with the case in which Poisson equation is solved only inside the semiconductor, we find that even if the static I–V characteristics remain practically unchanged, important differences appear in the dynamic and noise behaviour, reflecting the influence of an additional capacitance.

1. Introduction

With the aim of increasing the cut-off frequency of transistors, its gate length, L_g, has been reduced to the technological limit. However, this scaling process has the drawback that the parasitic gate resistance, r_g, increases proportionally to $1/L_g$, thus deteriorating the transconductance and, consequently, other important figures of merit of the devices like current gain and noise figure. Accordingly, while decreasing L_g, the value of the parasitic gate resistance must be kept as low as possible. A good compromise between these two requirements is the use of the T-gate technology [1–3], which allows us to have a short L_g (corresponding to the base of the T) with a low value of r_g, similar to that associated with a longer gate (corresponding to the head of the T). The wider is the head of the T-gate the lower is r_g, but at the same time the gate capacitance increases [3], therefore the width of the T-gate head must be chosen as a trade-off value between low resistance and low capacitance. The use of the recessed geometry to improve the device characteristics is also widespread. All these refinements lead to a rather complex configuration, whose simulation must include not only the transport inside the semiconductor, but also its capacitive coupling with the T-gate taking place through the dielectric (generally silicon nitride) used to passivate the devices.

Usually Monte Carlo (MC) simulations of MESFETs and HEMTs only consider the transport and electric field in the semiconductor [4–8] (taking as boundary conditions the reflection of the carriers and zero normal electric field at the limits of the simulation domain). Even if the dielectric is taken into account in some works [9, 10], it is not enough, since the head of the T-gate provokes a capacitive coupling between gate and semiconductor. This effect must be considered for having a completely realistic simulation, since it affects considerably the distribution of the electric field inside the device. In this paper we will show the differences which appear when the complete simulation is performed in the case of a 0.1 μm recessed gate δ-doped AlInAs/GaInAs HEMT. While the static I–V characteristics are practically the same as those obtained with the standard simulations, the dynamic and noise behaviour is affected by the influence of an additional capacitance.

The paper is organized as follows. In section 2 a summary of the simulation model is given. In section 3 the geometries of the simulated and fabricated HEMTs are presented and their main features are described. Then, in section 4 a comparison is performed between the results obtained from the MC simulation when the T-gate is taken into account or not. Values for the I–V characteristics, small signal equivalent circuit elements, P, R and C noise parameters and minimum noise figure will be given, thus performing a complete evaluation of the static, dynamic and noise performance of the devices. Finally, in section 5, we draw the main conclusions of this work.

0268-1242/99/090864+07$30.00

2. Monte Carlo simulation

For the calculations we use a semiclassical ensemble MC simulator self-consistently coupled with a 2D Poisson solver (finite-difference scheme, LU decomposition method) which allows the resolution of the potential in complicated geometries and non-uniform meshes. The boundary conditions for the inclusion of different dielectric materials, surface potential and T-gate will be explained later. Three non-parabolic spherical valleys (Γ, L and X) with ionized impurity, alloy, polar and non-polar optical phonon, acoustic phonon and intervalley scattering mechanisms are taken into account. Material parameters for the $Al_{0.48}In_{0.52}As$ and $Ga_{0.47}In_{0.53}As$ are reported in [11].

The devices are divided into meshes 50 Å long and 10 to 100 Å wide depending on the doping and the required resolution of the potential along the structure. They are simulated at 300 K during a number of time steps (1 fs each) ranging from 20 000 for the evaluation of the I–V characteristics to 200 000 for the noise calculations. Ohmic boundary conditions are considered in the source and drain contacts, which are placed vertically adjacent to different materials. Accordingly, nonuniform potential and concentration profiles are considered along these contacts: those that would be obtained if real top electrodes were simulated [5, 11–13]. The effect of degeneracy has been introduced by using locally the classical rejection technique, where the electron heating and nonequilibrium screening effects are introduced by using the local electron temperature [11, 14]. No other quantum effect is considered in the simulation. The validity of this approximation (mainly under high field conditions) and that of the whole Monte Carlo model has been confirmed in a previous work [11].

Let us focus now on the boundary conditions used for the Poisson solver, which are of great importance for the simulation of the T-gate geometry:

(a) A static charge is placed in the surface of the semiconductor in order to model the effect of its surface potential (which pins the Fermi level close to the middle of the energy gap). The boundary condition associated with this surface charge is:

$$\varepsilon_1 E_1 - \varepsilon_2 E_2 = \sigma_{12} \tag{1}$$

ε_i and E_i being the permittivity and the electric field normal to the surface, respectively, of the material labelled *i* (which can be the semiconductor, the dielectric or the air). σ_{ij} is the surface charge associated with the interface between the semiconductor and the dielectric/air, whose value on the cap layer is different to that on the bottom of the recess [11].

(b) When there is no surface charge at the interfaces (i.e. between two different dielectric materials) the continuity of the displacement vector normal to the surface is imposed:

$$\varepsilon_1 E_1 = \varepsilon_2 E_2. \tag{2}$$

(c) At the source, drain and gate contacts a fixed potential (Dirichlet condition), non-uniform in the case of the source and drain electrodes, is considered.

(d) At the limits of the simulation domain the usual von Neumann condition $E_i = 0$ is applied.

All these boundary conditions are included in the total system of equations, together with the standard Poisson equation for the nodes of the grid not at the boundaries, and then solved at each time step by using the LU decomposition method. This is a very efficient method, since the calculation of the inverse of the matrix representing the system of equations (which is the most time-consuming computation) is only performed once at the beginning of the simulation. Thus, only the calculation of the charge density and its product by the previously calculated inverse matrix must be done every time step.

The effect of the surface potential at the cap and recess surfaces of the device is modelled through a fixed negative surface charge (which is a good approximation at low biasing [5, 7–13]) that provokes carrier depletion in its surroundings. The value of the surface charge is not the same in the whole device, since in the bottom of the recess the interface material is AlInAs, while in the rest it is GaInAs. These two values of the surface charge will be taken as adjustable parameters that allow the fitting of the experimental I–V characteristics [9–13]. The value of the charge placed at the top of the cap layer, Q_c, affects the slope of the I–V characteristics, which decreases when Q_c is higher due to the increase of the total device resistance (without affecting the saturation level of drain current). In contrast, the increase of the surface charge at the bottom of the recess, Q_r, reduces the maximum drain current, since the width of the channel is decreased by the effect of the surface charge. Anyway, the influence of Q_r only appears under high gate voltages, since in the near pinch-off region the channel width depends only on V_{gs} (the negative gate bias is much stronger than the surface potential). Therefore, the value that we obtain for the threshold voltage is practically independent of the values of the surface charges, and is related almost exclusively to the semiconductor layer distribution under the gate.

More details about the consideration of the contact resistances [15], the transient simulation and small signal equivalent circuit extraction [10, 16, 17], the calculation of correlation functions, spectral densities, P, R and C noise parameters, intrinsic minimum noise figure [5, 18–22] and other details of the MC simulation can be found elsewhere [11–13, 23].

3. Device structure

The SEM photographs of the cross section of a real 0.1 μm recessed-gate δ-doped HEMT fabricated at the IEMN shown in figure 1(*a*) outline the geometry of the usual recessed T-gate configuration [2, 3]. The layer structure of this HEMT, which has been reproduced in the simulation, has already been presented in [11] and consists of an InP substrate, a 3000 Å $Al_{0.48}In_{0.52}As$ buffer followed by a 250 Å thick $Ga_{0.47}In_{0.53}As$ channel, three layers of $Al_{0.48}In_{0.52}As$ (a 50 Å spacer, a 5×10^{12} cm^{-2} δ-doped layer modelled as a 50 Å layer doped at $N_D = 10^{19}$ cm^{-3} and a 100 Å Schottky layer) and finally a 100 Å thick $Ga_{0.47}In_{0.53}As$ cap layer ($N_D = 5 \times 10^{18}$ cm^{-3}). Note also the presence of two air islands inside the recess, one at each side of the gate, which will be

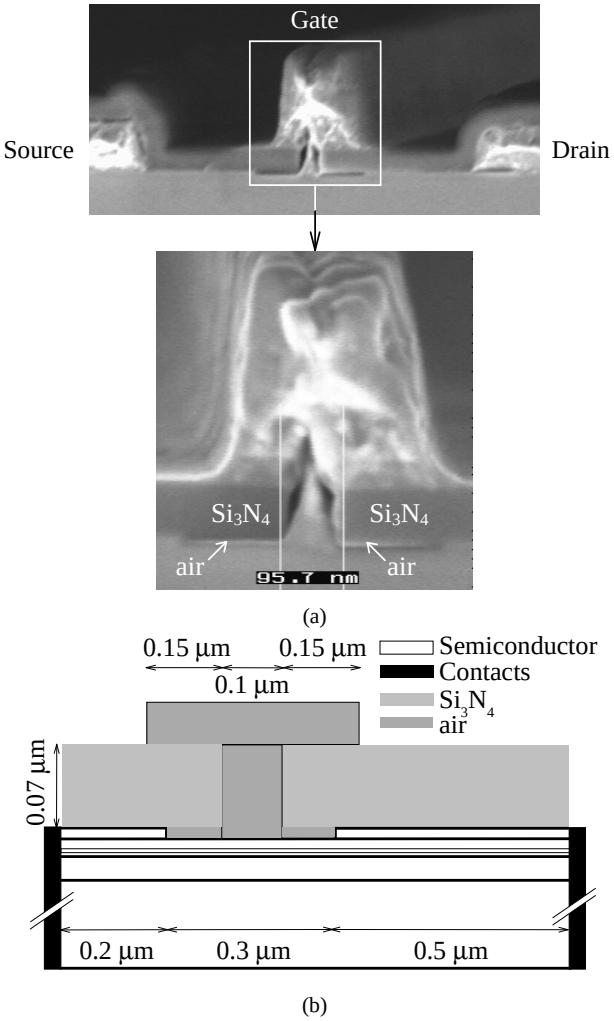

Figure 1. SEM photograph of the cross section of a real recessed T-gate HEMT (*a*) and its simplified representation used for the MC simulation (*b*).

also considered in the simulation. This dielectric disposition originates from the selective wet etching (using succinic acid), which just suppresses the GaInAs cap layer, being sharply stopped by the AlInAs Schottky layer (only 2–3 nm are removed). Indeed, the simulated devices, sketched in figure 1(*b*), have exactly the same layer distribution as that of the real HEMT shown before and almost the same geometry. The vertical position of the source and drain contacts does not introduce any significant change in the results. The non-simulated ohmic source region is considered in a post-processing stage by adding an extra value to the resistance of the source contact [11]. The rest of the features of the real HEMTs have been reproduced as closely as possible (the trapezoidal shape of the T-gate foot and the non-vertical edges of the recess have been simplified to rectangular features, but this does not significantly affect the electric field distribution).

Two different types of MC simulation will be performed. In the simplest one the simulation domain includes only the semiconductor, thus solving the Poisson equation by applying the usual boundary conditions at the interfaces, equations (1)

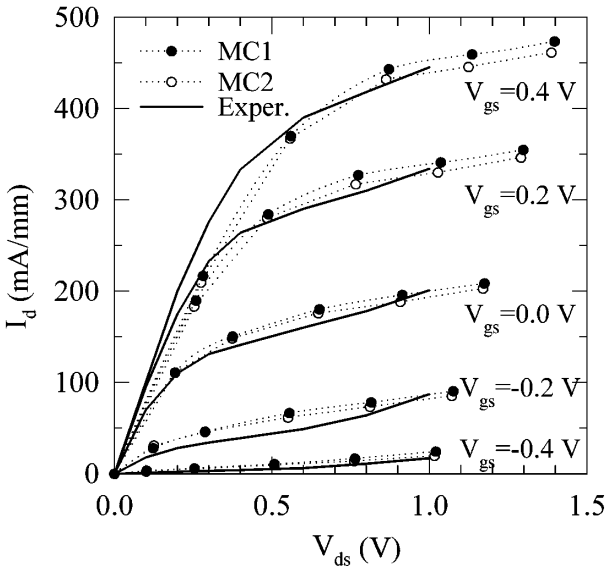

Figure 2. Comparison of the I–V characteristics measured in a real HEMT (solid line) with those obtained from the Monte Carlo simulations (dotted lines): MC1 (black circles) and MC2 (white circles).

and (2), and considering as negligible the normal electric field outside the semiconductor ($E_2 = 0$). The second type of simulation takes into account the different dielectric materials (silicon nitride and air) and the T shape of the gate contact by solving the Poisson equation not only inside the semiconductor but in the whole device structure (shown in figure 1(*b*)). These two different types of simulation will be called in the following MC1 (only semiconductor) and MC2 (whole structure).

4. Results

4.1. Static characteristics

The I–V characteristics of the real and simulated HEMTs are shown in figure 2. By adjusting separately the surface charge at the cap layer and at the bottom of the recess (whose values are $Q_c = -6.2 \times 10^{12}$ cm^{-2} and $Q_r = -4.3 \times 10^{12}$ cm^{-2}, respectively [11]) the static I–V characteristics of the real HEMT have been reproduced quite closely. The value of Q_c corresponds to an ideal surface potential of -0.5 V, while that of Q_r cannot be associated with a 'bulk' surface potential since it is placed on a non-doped material. The simulated threshold voltage is the same in both MC simulations ($V_T \approx -0.45$ V), and it is practically independent of the value of the surface charges. Indeed, it is in quite good agreement with both theoretical predictions ($V_T \approx -0.48$ V) [8] and experimental measurements ($V_T \approx -0.50$ V). In figure 2 we can also appreciate that impact ionization begins to be significant at $V_{ds} > 0.8$ V, increasing the slope of the curves and worsening the agreement with the simulations (where this process is not taken into account). This effect could be somewhat diminished by increasing the extension of the recess towards the drain (thus lowering the electric fields in that region). Anyway, in order to obtain the lowest

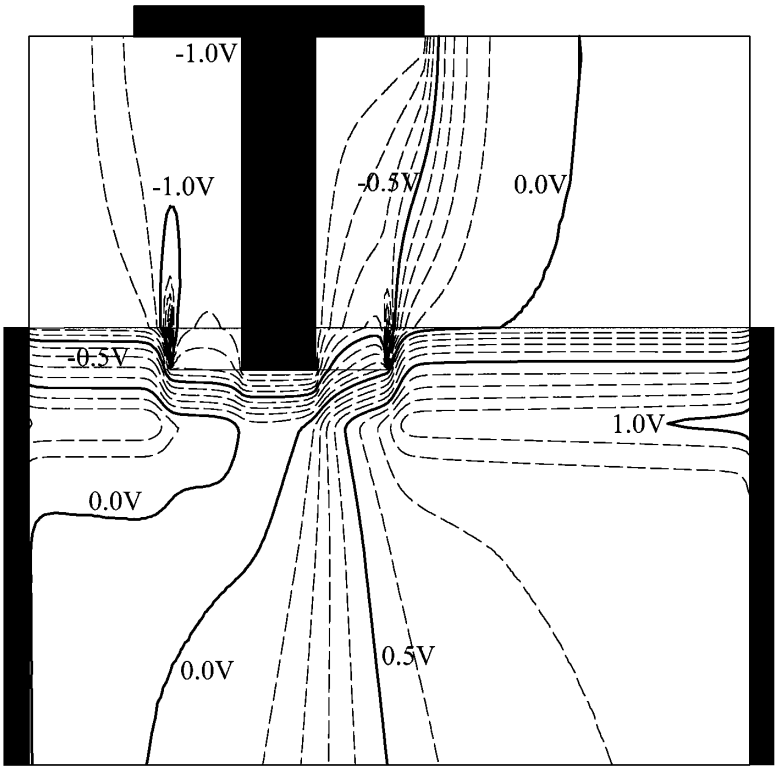

Figure 3. Equipotential lines for an intrinsic biasing of $V_{ds} = 0.75$ V, $V_{gs} = -1.0$ V (extrinsic biasing of $V_{ds} = 0.79$ V, $V_{gs} = -0.27$ V) obtained with the complete Monte Carlo simulation (MC2). Labels indicate the electric potential taking as reference the potential in the substrate at the source contact.

noise conditions, we will never use such drain biases, thus avoiding any influence of impact ionization. It can be also observed in figure 2 that both types of MC simulation lead to similar values of the I_d, with only a little decrease of current in the case of MC2 with respect to MC1. This is an expected result since the drain current value is mainly determined by the maximum depth of the depletion region under the gate, which is essentially affected by the value of the applied gate potential, regardless of the T shape of this electrode. Nevertheless, the electric field profile obtained inside the semiconductor presents significant differences depending on the type of simulation used. The equipotential lines in the simulation domain calculated within the scheme MC2 are shown in figure 3. The intrinsic bias point is $V_{ds} = 0.75$ V, $V_{gs} = -1.0$ V, which gives a drain current of 60.9 A m^{-1} (in the near pinch-off region, where noise characteristics are optimum). Taking into account the source and drain contact resistances and the Schottky barrier, the corresponding extrinsic bias point is, approximately, $V_{ds} = 0.79$ V, $V_{gs} = -0.27$ V. In figure 3 it can be observed how the equipotential head of the T-gate influences the distribution of the potential inside the dielectrics (silicon nitride and air). As we shall see in the following, this influence even penetrates into the semiconductor area under the recess. The change in the curvature of the equipotential lines (reflecting the discontinuity of the normal electric field) observed at the boundary between the two dielectrics is just due to the different dielectric constant of each material (equation (2)), while at the dielectric–semiconductor boundaries it is also affected by the presence of the surface charge (equation (1)).

In order to demonstrate the differences between the two simulation schemes, we show in figure 4 the electric potential, vertical field (positive in direction to the gate) and electronic concentration at the top of the GaInAs channel layer obtained with MC1 and MC2, and their difference (represented only in the region near the gate, just where MC1 and MC2 do not give identical results). The bias point is the same as in figure 3. The main difference appearing when the T-gate geometry is considered is a decrease in the potential in the semiconductor regions under the flanks of the T-gate head (figure 4(*a*)) due to the influence of the negative gate potential applied to the gate, which is not completely shielded by the presence of the dielectric between the gate head and the semiconductor. This effect takes place mainly in the regions below the part of the recess that is not in contact with the gate electrode. Moreover, the difference between MC1 and MC2 is more pronounced at the drain side of the gate, since the potential drop from gate to drain is much higher than from gate to source. The influence of the T-gate on the potential distribution leads also to a different profile of the vertical electric field, figure 4(*b*), which is stronger in MC2 at both sides of the gate foot, thus pushing down the electrons and depleting more efficiently those regions, figure 4(c). Therefore, the main difference between MC1 and MC2 is the horizontal enlargement of the depletion region under the gate, thus increasing slightly the effective gate length. This effect is at the origin, on the one hand, of the small decrease in the drain current obtained with MC2 with respect to MC1 observed in figure 2 (the total resistance of the device is increased due to the reduction of the channel width at both sides of the gate), and, on the

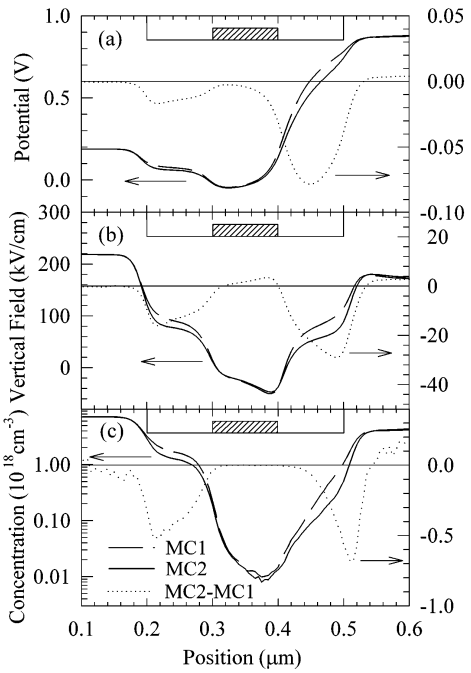

Figure 4. Potential (*a*) vertical electric field (*b*) and electron concentration (*c*) at the top of the GaInAs channel layer obtained from MC1 (dashed line, left axes), MC2 (solid line, left axes) and its difference (dotted line, right axes), represented only near the recess as a function of the longitudinal position. The biasing is the same as in figure 3.

other hand, of the increase in the gate capacitance (the space-charge region under the gate is enlarged by the presence of the T-gate). This last effect will be addressed in the next section related to the study of the dynamic behaviour of our device.

4.2. Dynamic behaviour

The different distribution of carriers and electric potential leads also to differences in the small signal behaviour of the devices. The capacitive coupling between the head of the T-gate and the semiconductor must have some influence on the capacitive elements of the small signal equivalent circuit associated with the gate. To detect this influence, we evaluate the intrinsic small signal equivalent circuit of the transistor, taking as a basis the Y parameters calculated by means of the Fourier analysis of the transient response of the transistor to voltage steps applied in the gate and drain electrodes [10, 17].

The values of the different capacitances (gate–source, C_{gs}, drain–source, C_{ds}, and gate–drain, C_{gd}) as a function of the drain current are shown in figure 5 for an extrinsic drain voltage of 0.8 V. As expected, the value of C_{ds} is similar for MC1 and MC2 since this parameter represents the coupling between source and drain taking place mainly through the carriers in the buffer, which practically are not affected by the inclusion of the T-gate. Also, the

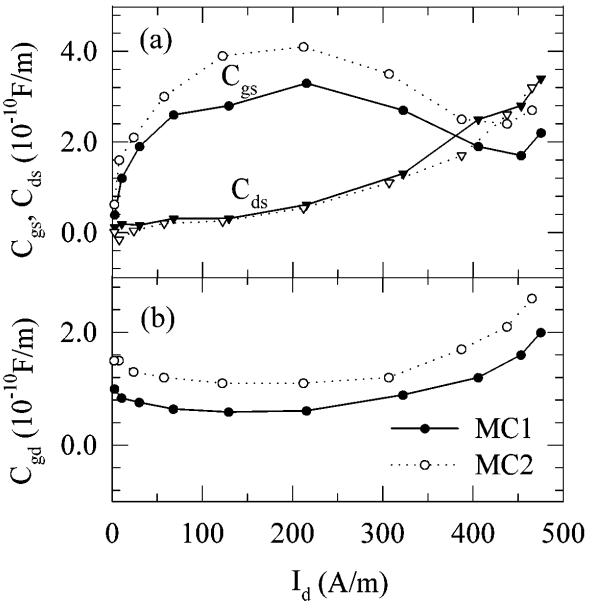

Figure 5. Capacitive elements of the intrinsic small signal equivalent circuit: (*a*) gate–source, C_{gs}; drain–source, C_{ds}; and (*b*) gate–drain, C_{gd}, as a function of the drain current for an extrinsic bias $V_{ds} = 0.8$ V. The results are obtained from MC1 (solid line, black circles) and MC2 (dotted line, white circles).

rest of parameters of the small signal equivalent circuit [17] remain practically unchanged: transconductance, drain conductance (both due to the quasi-invariance of I–V characteristics, figure 2), source-channel resistance and transit time. However important differences appear in the values of C_{gs} and C_{gd}. They show a significant increase when the capacitive coupling between the gate and the semiconductor (through the dielectric) is taken into account in MC2. This increase in C_{gs} and C_{gd} agrees very well with the addition of a capacitor (connected in parallel with the gate) whose plates are the head flank of the gate at the side of the corresponding electrode and the semiconductor below it. The theoretical value of this capacitance is 0.78×10^{-10} F m^{-1} (the same at each side of the gate).

4.3. Noise behaviour

Once static and dynamic characteristics have been determined, we will perform the study of the noise behaviour of the device. In order to characterize the noise performance of real devices the most commonly used parameter is the intrinsic minimum noise figure, F_{min} [1, 5, 21, 22]. It indicates the amount of noise power that an active device introduces in the signal which is amplifying, but it does not give information about the origin of the noise. To this end we will also make use of a complementary noise representation through the P, R and C noise parameters. P is the parameter related to the drain noise, R to the gate noise and C is the imaginary part of the correlation coefficient. The higher are P and R, and the lower is C, the more noisy is the device and the higher is F_{min} [5, 20, 21].

Figure 6 shows the intrinsic values of F_{min}, P, R and C as a function of the drain current at 10 GHz (F_{min} also for 94 GHz) for an extrinsic drain voltage of 0.8 V. It can be

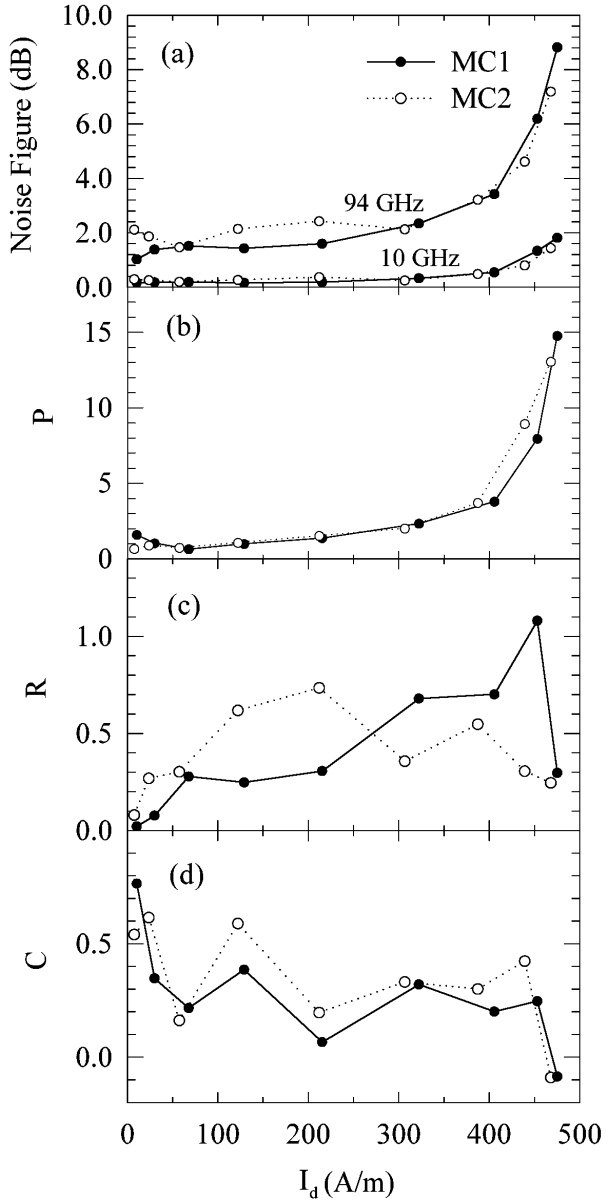

Figure 6. (*a*) Minimum intrinsic noise figure at 10 and 94 GHz, and (*b*) P, (*c*) R and (*d*) C noise parameters at 10 GHz as a function of the drain current for an extrinsic bias $V_{ds} = 0.8$ V. The results are obtained from MC1 (solid line, black circles) and MC2 (dotted line, white circles).

noticed that in the range of low and intermediate currents the value of F_{min} obtained from MC2 is higher than that obtained from MC1 (figure 6(*a*)). Moreover, we can appreciate the increase of F_{min} with the frequency, leading also to a larger difference between MC1 and MC2. In addition to this, P, R and C parameters give us additional information. The drain noise (P) and the gate–drain correlation (C) are similar in MC1 and MC2, but the gate noise increases when the T-gate is considered, mainly at low currents (which are just the typical low noise biasing conditions). Consequently, the increase of F_{min} can be related to the higher gate noise, both associated with the increase of the gate capacitance (figure 5) and with the decrease of the cut-off frequency of the device in the presence of the T-gate.

Therefore, independently of the noise representation, we conclude that it is necessary to take into account the effect of the T-gate when analysing the noise of the devices. This is because the noise depends strongly on the dynamic behaviour, where the effect of the capacitive coupling between the head of the gate and the transport in the semiconductor is very significant.

We must stress that we have only considered the influence of the T-gate on the intrinsic F_{min}, without taking into account the associated lower value of the gate resistance, which strongly affects the extrinsic F_{min}. Thus, although the gate capacitance of the T-gate deteriorates the intrinsic F_{min}, the reduction of the gate resistance would lead to a lower extrinsic noise.

5. Conclusions

Taking as a basis the geometry and parameters of a real structure, and using an MC simulation, we have performed a realistic simulation of a 0.1 μm gate length AlInAs/GaInAs, InP based HEMT. The effect of the T-gate on the dynamic behaviour and noise performance of recessed gate δ-doped HEMTs has been analysed. To this end, two different MC simulations have been used, with and without considering the T-gate configuration and the dielectrics, and thus their corresponding influence on the electric field inside the semiconductor. We have found that the effect of the T-gate on the potential distribution leads to an enlargement (towards drain and source) of the depletion region under the gate. This provokes a small decrease of the current (I–V characteristics only change slightly) and also a significant increase of the gate capacitance. This second effect comes out clearly when the small signal circuit parameters are calculated, revealing that gate–drain and gate–source capacitances are increased due to the capacitive coupling between the head of the gate and the semiconductor. To complete the device characterization noise calculations have been performed. Since noise and dynamic behaviours are closely related, the increase of the gate capacitance leads to the increase of the gate noise (R parameter) and, consequently, of the minimum noise figure.

Acknowledgments

This work was supported partially by the projects SA44/99 from the Consejería de Educación y Cultura de la Junta de Castilla y León and PB97-1331 from the Dirección General de Enseñanza Superior e Investigación Científica.

References

[1] Onodera K, Nishimura K, Aoyama S, Sugitani S, Yamane Y and Hirano M 1999 Extremely low-noise performance of GaAs MESFET's with wide-head T-shaped gate *IEEE Trans. Electron Devices* **46** 310

[2] Wang G W, Chen Y K, Schaff W J and Eastman L F 1988 A 0.1 μm gate $Al_{0.5}In_{0.5}As/Ga_{0.5}In_{0.5}As$ MODFET fabricated on GaAs substrates *IEEE Trans. Electron Devices* **35** 818

[3] Nguyen L D, Brown A S, Thompson M A and Jelloian L M 1992 50-nm self-aligned-gate pseudomorphic AlInAs/GaInAs high electron mobility transistors *IEEE Trans. Electron Devices* **39** 2007
[4] Jensen G U, Lund B, Fjeldly T A and Shur M 1991 Monte Carlo simulation of short-channel heterostructure field effect transistors *IEEE Trans. Electron Devices* **38** 840
[5] Mateos J, González T, Pardo D, Tadyszak P, Danneville F and Cappy A 1998 Noise analysis of 0.1 μm gate MESFETs and HEMTs *Solid-State Electron.* **42** 79
[6] Dollfus P, Bru C and Hesto P 1993 Monte Carlo simulation of pseudomorphic InGaAs/GaAs high electron mobility transistors: physical limitations at ultrashort gate length *J. Appl. Phys.* **73** 804
[7] Kim K W, Tian H and Littlejohn M A 1991 Analysis of delta-doped and uniformly doped AlGaAs/GaAs HEMTs by ensemble Monte Carlo simulations *IEEE Trans. Electron Devices* **38** 1737
[8] Kizilyalli I C, Artaki M and Chandra A 1991 Monte Carlo study of GaAs/Al_xGa_{1-x}As MODFETs: effects of GaAs/Al_xGa_{1-x}As composition *IEEE Trans. Electron Devices* **38** 197
[9] Babiker S, Asenov A, Barker J R and Beaumont S P 1996 Finite element Monte Carlo simulation of recess gate compound FETs *Solid-State Electron.* **39** 629
[10] Babiker S, Asenov A, Cameron N, Beaumont S P and Barker J R 1998 Complete Monte Carlo RF analysis of 'real' short channel compound FETs *IEEE Trans. Electron Devices* **45** 1644
[11] Mateos J, González T, Pardo D, Hoel V and Cappy A 1999 Improved Monte Carlo algorithm for the simulation of δ-doped AlInAs/GaInAs HEMTs *IEEE Trans. Electron Devices* at press
[12] Mateos J, González T, Pardo D, Tadyszak P, Danneville F and Cappy A 1997 Noise and transit time in ungated FET structures *IEEE Trans. Electron Devices* **44** 2128
[13] Mateos J, González T, Pardo D, Tadyszak P, Danneville F and Cappy A 1998 Influence of Al mole fraction on the noise performance of GaAs/Al_xGa_{1-x}As HEMTs *IEEE Trans. Electron Devices* **45** 2081
[14] Miranda Pantoja J M and Sebastián Franco J L 1997 Monte Carlo simulation of electron velocity in degenerate GaAs *IEEE Electron Device Lett.* **18** 258
[15] Babiker S, Asenov A, Cameron N and Beaumont S P 1996 Simple approach to include external resistances in the Monte Carlo simulation of MESFETs and HEMTs *IEEE Trans. Electron Devices* **43** 2032
[16] Dambrine G, Cappy A, Heliodore F and Playez E 1988 A new method for determining the FET small-signal equivalent circuit *IEEE Trans. Microwave Theory Technol.* **32** 1151
[17] González T and Pardo D 1995 Monte Carlo determination of the intrinsic small-signal equivalent circuit of MESFETs *IEEE Trans. Electron Devices* **42** 605
[18] Varani L, Reggiani L, Kuhn L, González T and Pardo D 1994 Microscopic simulation of electronic noise in semiconductor materials and devices *IEEE Trans. Electron Devices* **41** 1916
[19] González T, Pardo D, Varani L and Reggiani L 1995 Monte Carlo analysis of the behavior and spatial origin of electronic noise in GaAs MESFETs *IEEE Trans. Electron Devices* **42** 991
[20] Cappy A 1988 Noise modelling and measurement techniques *IEEE Trans. Microwave Theory Technol.* **36** 1
[21] Pucel R A, Haus H A and Statz H 1974 Signal and noise properties of gallium arsenide field effect transistors *Adv. Electron. Electron Phys.* **38** 195
[22] Rothe H and Dahlke W 1956 Theory of noisy fourpoles *Proc. IRE* **44** 811
[23] González T and Pardo D 1996 Physical models of ohmic contact for Monte Carlo device simulation *Solid-State Electron.* **39** 555