Monte Carlo Study of the Dynamic Performance of a 100-nm-Gate InAlAs/InGaAs Velocity Modulation Transistor

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***Abstract*—We report a Monte Carlo study of the dynamic behavior of an InAlAs/InGaAs velocity modulation transistor (VMT) based on the topology of a double-gate high electron mobility transistor (DG HEMT), which is a HEMT with two opposite gates controlling the carrier flow through the conducting channel. In the VMT, the source and drain electrodes are connected by two channels with different mobilities, and electrons are transferred between both by changing the gate voltages in differential mode (DM). As a result, the drain current is modulated while keeping the total carrier density constant, thus, in principle, avoiding capacitance charging/discharging delays. However, the low values taken by the transconductance, as well as the high capacitance between the two gates in DM operation, lead to a deficient dynamic performance.**

***Index Terms*—Double-gate high electron mobility transistor (DG HEMT), dynamic behavior, Monte Carlo (MC) simulations, velocity modulation transistor (VMT).**

I. Introduction

InP-BASED high electron mobility transistors (HEMTs) have proven to exhibit an excellent performance for applications in the microwave and millimeter-wave frequency ranges [1]. To further improve their behavior, alternative solutions based on an evolution of the standard HEMT design have been proposed [2]–[6]. Thus, the double-gate (DG) HEMT, which is a HEMT with two gates placed on each side of the conducting InGaAs channel, has been recently fabricated. The progress of the DG-HEMT technology allows the design and fabrication of III-V velocity modulation transistors (VMTs) [7]. In VMTs [8]–[14], the source and drain electrodes are connected by two channels with different mobilities μ, whereas two gates allow the control of the global electron density n_T. Electrons can be shifted between the two channels by changing the gate voltages in differential mode (DM). Due to the different transport properties in the two channels, the drain current I_D is modified while keeping n_T constant, i.e., by velocity modulation. In this way, it is, in principle, possible to overcome the transit-time limit for high-frequency operation. The aim of this work is to perform a deep analysis of a 100-nm-gate InAlAs/InGaAs VMT by means of a 2-D Monte Carlo (MC) simulator [15], [16], which provides a full microscopic interpretation of the static and dynamic performances of the VMT. Simulations show that the cutoff frequencies take values that are much lower than predicted [8] because of the low transconductance g_m associated to the VM behavior and the high geometrical capacitance appearing between the two gate electrodes when operating in DM.

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II. Physical Model

For the calculations, we make use of a semiclassical ensemble MC simulator self-consistently coupled with a 2-D Poisson solver whose validity has been proven for standard [15]–[17] and DG [5], [6] HEMTs by reproducing their experimental static and dynamic behaviors. In addition, our model has been successfully applied to the study of the static behavior of a fabricated VMT [7]. The MC simulator takes into account important physical effects, such as the influence of degeneracy in the electron accumulation appearing in the channel, implemented by means of the rejection technique [15], [16].

In order to establish a comparison with a real transistor, the topology of the VMT under study, which is plotted in Fig. 1(a), is very similar to that of the fabricated device [7]. Unintentional defects originated in the technological process have not been taken into account, as the gate contact is not covering the whole mesa, which degrades the pinchoff behavior. In addition, the source region, which is essentially ohmic, has been reduced (with its effect introduced as a resistance in a postprocessing stage). The active layer structure and the technological process for the fabrication of the VMT were detailed in [7]. Two opposite 100 nm-gate electrodes control the total electron density in the channels and the carrier shift between them in DM operation. The only difference with respect to a DG-HEMT [2]–[6] is that the channel is divided into two regions, i.e., a high-μ undoped channel (channel 1) and a low-μ channel with compensated doping (channel 2). The compensated doping allows increasing the ionized impurity scattering and, thus,

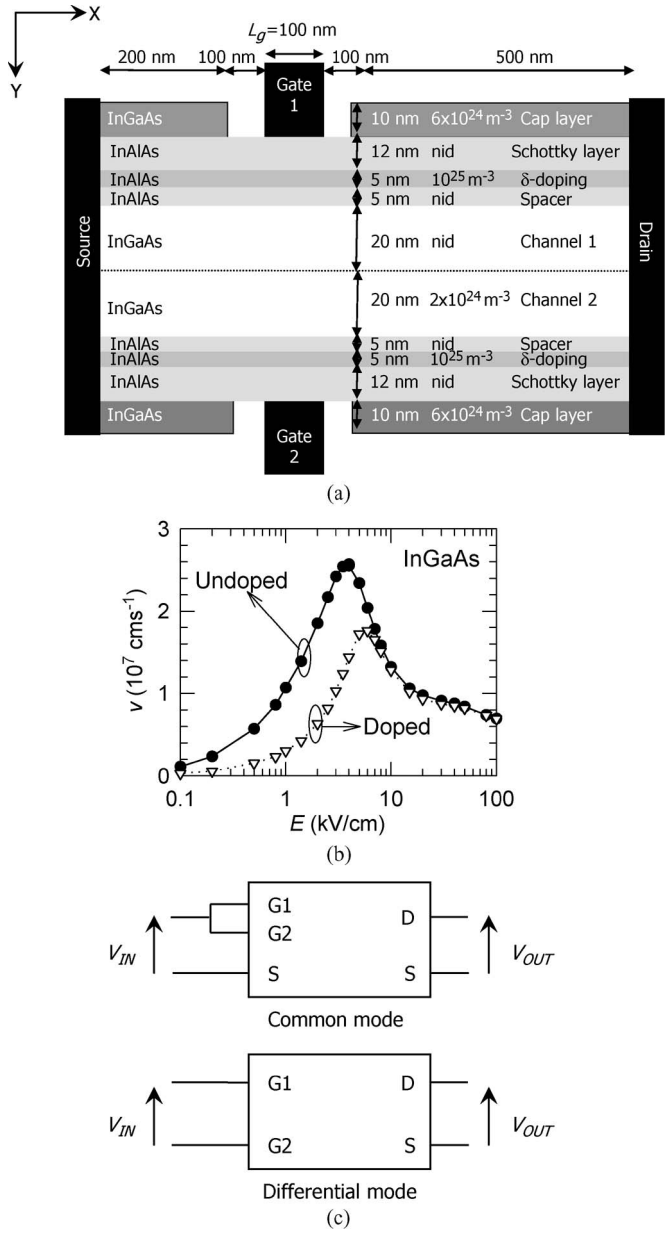

Fig. 1. (a) Schematic topology of the simulated 100-nm-gate VMT. (b) Electron velocity versus electric field for the undoped and 2×10^{18} cm^{-3}-doped bulk InGaAs. (c) Schematic representation of the CM and DM biasing.

decreasing the electron mobility. At room temperature, the calculated low-electric-field mobilities in the high-μ and low-μ channels are $\sim$12000 cm^2/V $\cdot$ s and $\sim$2700 cm^2/V $\cdot$ s, respectively. ($\sim$10000 cm^2/V $\cdot$ s and $\sim$2600 cm^2/V $\cdot$ s were measured by Hall effect on experimental structures [7], respectively.) The electron velocity versus electric field curves for the materials in both channels are shown in Fig. 1(b).

In order to perform the dc analysis of the proposed VMT, we define the gate voltages by means of two terms, i.e., a common-mode (CM) bias voltage $V_{\rm GOFF}$, which controls the level of depletion under both gates and allows adjusting the total electron density in the channel n_T (and, therefore, the drain current level), and a differential potential $V_{\rm GDIFF}$ that modulates the population of the high-μ and low-μ channels. Then, the dc gate voltages are $V_{G1S} = V_{\rm GOFF} + V_{\rm GDIFF}/2$ and $V_{G2S} = V_{\rm GOFF} - V_{\rm GDIFF}/2$. The VMT can operate in CM ($V_{\rm GDIFF} = 0$) and in DM ($V_{\rm GDIFF} \neq 0$) [see Fig. 1(c)]. The CM dynamic behavior of the VMT is determined by means of the standard intrinsic small-signal equivalent circuit (SSEC) of FETs [18]. It is calculated by taking as a basis the Y-parameters, which are obtained by using the typical MC technique [19]. However, the dynamic analysis of the VMT differential behavior, still controversial, requires to define appropriately the DM input potential and current, which are typically $V_{\rm IN} = V_{\rm GDIFF} = V_{G1S} - V_{G2S}$ and $I_{\rm IN} = (I_{G1} - I_{G2})/2$, respectively [20]. Thus, the input voltage is not referenced to the source.

In order to compare the CM and DM dynamic behavior of the VMT, an input capacitance $C_{\rm IN}$ is defined as ${\rm Im}[Y_{11}]/2\pi f$, where $Y_{11} = \Delta I_{\rm IN}/\Delta V_{\rm IN}$ when $V_{\rm DS}$ remains constant, and f is the operation frequency. $C_{\rm IN}$ can be generally considered as the addition of the gate-to-source $C_{\rm gs}$, gate-to-drain $C_{\rm gd}$, and gate1-to-gate2 C_{g1g2} capacitances. When operating in CM, $C_{\rm IN} = C_{\rm gs} + C_{\rm gd}$, because the two gates are short-circuited ($V_{G1S} = V_{G2S}$), so that C_{g1g2} has no influence, and $C_{\rm gs}$ and $C_{\rm gd}$ are determined as in [19]. When working in DM, $C_{\rm gs}$ and $C_{\rm gd}$ are almost zero since the amount of electrons under the gate remains nearly constant and there is no need for channel charging/discharging (as we will see in Section III). Thus, $C_{\rm IN}$ turns out to coincide practically with C_{g1g2}. The main contribution to C_{g1g2} is essentially geometrical (the free carrier contribution is much lower), so that the possible influence of the electron energy quantization normal to the channels [21, 22], which are neglected in our model, can be disregarded. The intrinsic cutoff frequency f_C can be calculated as $g_m/2\pi C_{\rm IN}$ in both operation modes. In order to account for the device parasitic elements, the extrinsic $f_{\rm max}$ and f_t, which are defined as the values for which Mason's unilateral power gain U and the short-circuit current gain H_{21}, respectively, go to 1, are then calculated. However, the inclusion of the parasitic elements is still uncertain when dealing with the DM operation since the SSEC is not well established yet, so that just the extrinsic resistances (extracted from the comparison between the experimental and MC results [7]) will be taken into account for the calculation of $f_{\rm max}$ and f_t.

III. Results

A. Static Behavior

Fig. 2 presents the experimental and MC extrinsic output characteristics of the VMT: (a) I_D–$V_{\rm DS}$ for $V_{\rm GDIFF} = 0$ V (CM) and (b) I_D–$V_{\rm GDIFF}$ for $V_{\rm DS} = 0.2$ V (DM), for different values of $V_{\rm GOFF}$. For the MC values, extrinsic contact resistances $R_S = 0.445\ \Omega \cdot$ mm and $R_D = 0.205\ \Omega \cdot$ mm have been considered. The agreement between experimental and MC results is very satisfactory in CM (at least up to $V_{\rm DS} =$ 0.3 V), whereas some differences arise in DM [7]. While in CM [Fig. 2(a)], the VMT works as a classic FET device (specifically as a DG-HEMT [2]–[6]). In DM operation, the values taken by I_D depend on $V_{\rm GDIFF}$ due to the velocity-modulation effect: when increasing $V_{\rm GDIFF}$, the electron density is transferred from the low-μ to the high-μ channel, thus increasing the drain

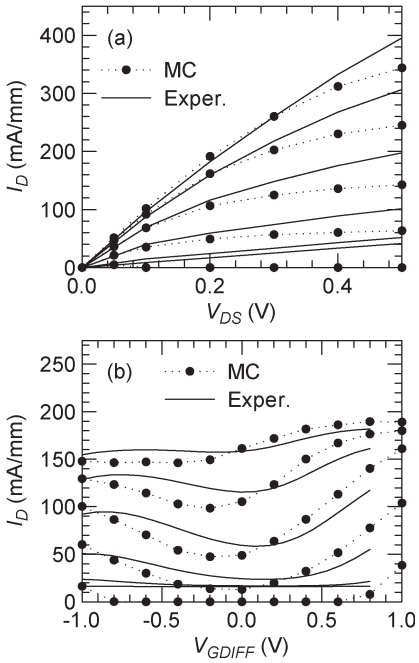

Fig. 2. Experimental and MC (a) I_D–$V_{\rm DS}$ for $V_{\rm GDIFF} = 0$ V and (b) I_D–$V_{\rm GDIFF}$ for $V_{\rm DS} = 0.2$ V, for the 100-nm-gate VMT. $V_{\rm GOFF}$ is 0 V for the top curves in (a) and -0.1 V for those in (b), and the potential step is $\Delta V_{\rm GOFF} = 0.1$ V.

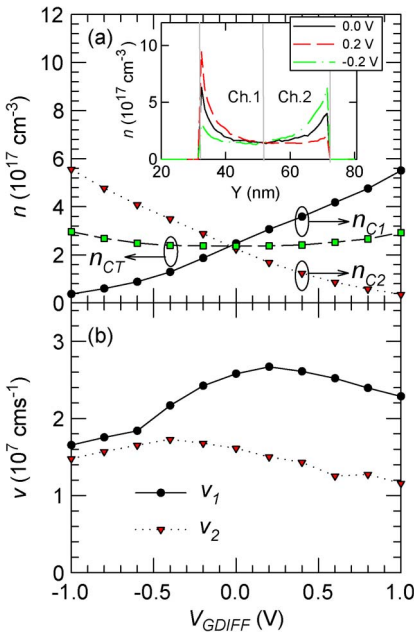

Fig. 3. (a) Mean electron density in the high-μ channel, n_1, in the low-μ channel, n_2, and in the whole channel, n_T, and (b) mean longitudinal electron velocity in both channels (high-μ v_1 and low-μ v_2), as a function of $V_{\rm GDIFF}$, for $V_{\rm DS} = 0.2$ V and $V_{\rm GOFF} = -0.1$ V. These values have been calculated in the region of the channel just below the gate contacts. (Inset) Transversal profile of electron concentration under the gate for different $V_{\rm GDIFF}$. The top gate is at the left, and the bottom gate at the right side of the graph. $V_{\rm DS} = 0.2$ V, and $V_{\rm GOFF} = -0.1$ V.

current. To clarify this behavior, Fig. 3 presents, as a function of $V_{\rm GDIFF}$, (a) the mean electron density in the high-μ channel n_{C1}, in the low-μ channel n_{C2}, and in the whole channel $n_{\rm CT}$, and (b) the mean electron velocity in both channels (high-μ v_{C1}, and low-μ v_{C2}), for $V_{\rm DS} = 0.2$ V and $V_{\rm GOFF} = -0.1$ V. These values have been calculated in the region of the channel below the gate contacts. For low values of $V_{\rm GDIFF}$ ($|V_{\rm GDIFF}| < 0.3$ V), $n_{\rm CT}$ practically does not change, corresponding to the VM behavior [7]. Fig. 3(b) confirms the enhanced mean electron velocity in the high-μ channel. To further illustrate the variation of the charge-accumulation regions in the channel with $V_{\rm GDIFF}$, the electron density profile along the vertical direction under the gate is shown in the inset of Fig. 3(a). All these facts corroborate that the behavior of I_D in DM observed in Fig. 2(b) for small values of $V_{\rm GDIFF}$ is actually due to velocity modulation and not to the variation of the electron population in the global channel.

However, some deviations from the ideal VMT behavior appear when increasing $|V_{\rm GDIFF}|$. An increase in I_D for the negative values of $V_{\rm GDIFF}$ is observed [Fig. 2(b)]. This is due to an increase in $n_{\rm CT}$ associated to the asymmetric dependence of the individual channel populations on $V_{\rm GDIFF}$, as can be noticed in Fig. 3(a). When increasing $V_{\rm GDIFF}$, the low-μ channel pinches off; therefore, even if n_{C1} increases linearly with $V_{\rm GDIFF}$, n_{C2} can no longer decrease, thus augmenting the global channel electron density. For negative values of $V_{\rm GDIFF}$, the same happens with exchanged channels. As a consequence, for high $|V_{\rm GDIFF}|$, the drain current variation is not entirely related to velocity modulation. These phenomena are more pronounced when $V_{\rm GOFF}$ decreases, because the global channel electron density at equilibrium is smaller. Moreover, in Fig. 3(b), it can also be observed that, instead of the expected constant values of electron velocity in each channel, a significant dependence on $V_{\rm GDIFF}$ is found, particularly for the high-μ channel. This dependence degrades the velocity modulation effect, mainly for negative $V_{\rm GDIFF}$, when the velocities in both channels tend to become similar. The observed dependence of the electron density and mean velocity on $V_{\rm GDIFF}$ leads to the U shape of the I_D–$V_{\rm GDIFF}$ characteristics, which is more noticeable at low $V_{\rm GOFF}$, where the linear region of pure velocity modulation (constant $n_{\rm CT}$ for low $V_{\rm GDIFF}$) is quite small.

In order to explain the dependence of the electron velocity on $V_{\rm GDIFF}$, Fig. 4 presents (a) v_1, (b) the mean horizontal electric field along the high-μ channel E_1, (c) v_2, and (d) the mean horizontal electric field along the low-μ channel E_2, for different values of $V_{\rm GDIFF}$. The position of the recess and the gates is also indicated. For $V_{\rm GDIFF} = 0$ V, the difference between v_1 and v_2 is confirmed. The profile of v_1 is strongly dependent on $V_{\rm GDIFF}$ [Fig. 4(a)]. In particular, when $V_{\rm GDIFF} = -0.6$ V ($V_{G1S} = -0.2$ V, $V_{G2S} = +0.4$ V), E_1 is positive in the channel region under the source side of the gate; thus, the value of v_1 is reduced with respect to the case of $V_{\rm GDIFF} = 0$ V and approaches v_2. In contrast, the dependence of the average v_2 on $V_{\rm GDIFF}$ is much weaker since the profile of v_2 is only slightly affected by the different distribution of the electric field in the low-μ channel [Fig. 4(c)]. Therefore, the particular values of v_1 and v_2, as well as the difference between them, depend on the electric field distribution and, thus, on the biasing.

B. Dynamic Behavior

Regarding the dynamic behavior of the device, a comparison between the DM and CM operations of the VMT is performed.

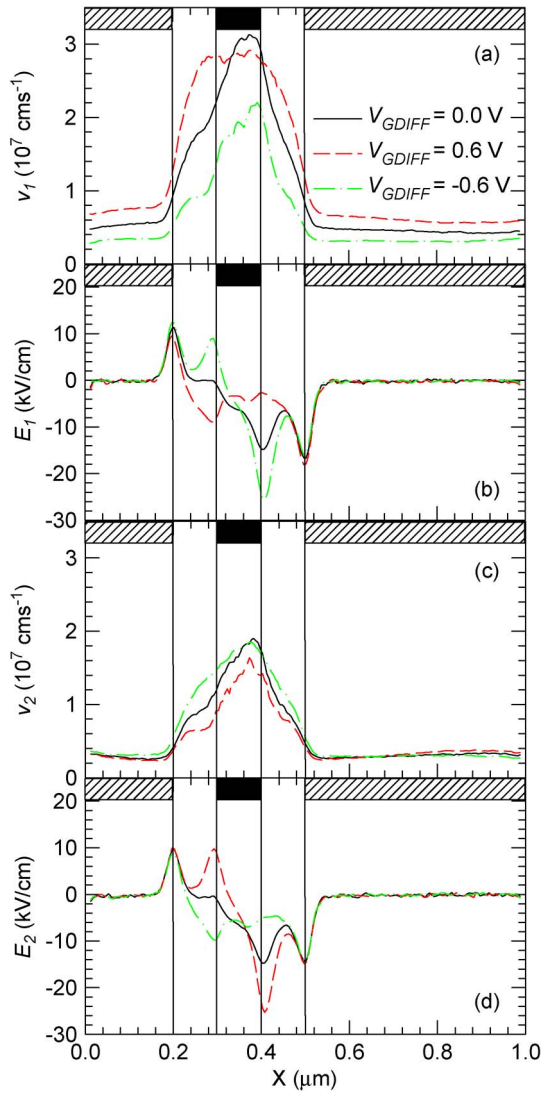

Fig. 4. Profiles of (a) and (c) longitudinal electron velocity and (b) and (d) mean electric field along the (a) and (b) high-μ channel and (c) and (d) low-μ channel, for $V_{\rm DS} = 0.2$ V, $V_{\rm GOFF} = -0.1$ V and several values of $V_{\rm GDIFF}$. The position of the gates and the recess is also indicated.

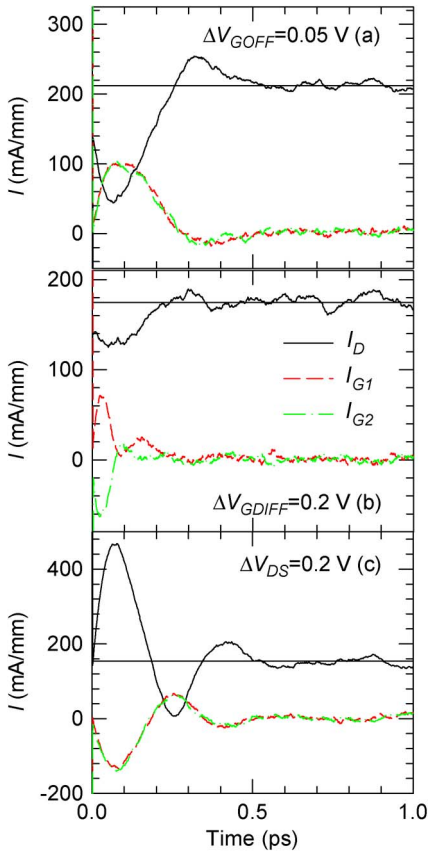

Fig. 5. Time evolution of I_D, I_{G1}, and I_{G2} when voltage steps of (a) $\Delta V_{\rm GOFF} = 0.05$ V (CM), (b) $\Delta V_{\rm GDIFF} = 0.2$ V (DM), and (c) $\Delta V_{\rm DS} = 0.2$ V are applied to the VMT terminals. The starting bias point is $V_{\rm DS} = 0.5$ V, $V_{\rm GOFF} = -0.2$ V, and $V_{\rm GDIFF} = 0$ V.

At the moment, due to technical difficulties, a proper high-frequency characterization of four-terminal (three-port) devices operating in DM cannot be done; thus, there are no available experimental results to establish a comparison. Fig. 5 presents the time evolution of I_D, I_{G1}, and I_{G2} when a voltage step of (a) $\Delta V_{\rm GOFF} = 0.05$ V (CM), (b) $\Delta V_{\rm GDIFF} = 0.2$ V (DM), and (c) $\Delta V_{\rm DS} = 0.2$ V is applied at time 0. Initially (at time $<$ 0), $V_{\rm DS} = 0.5$ V, $V_{\rm GOFF} = -0.2$ V, and $V_{\rm GDIFF} = 0$ V. The horizontal lines correspond to the final steady-state values of I_D, and they are included to estimate the transient time. The total current is the result of the addition of the conduction and the displacement currents, i.e., $I = I_{\rm con} + I_{\rm dis}$. In these figures, only $I_{\rm con}$ are noticeable since $I_{\rm dis}$ contributes only at the instant when the potential step is applied (and exceeds the represented current range). In CM, a change in the electron concentration under the gates takes place, corresponding to the classic field effect I_D modulation in FETs. In this case, as observed in Fig. 5(a), the steady-state values of currents (and channel population) are reached after a transient of about 0.6 ps. A similar behavior of the current is found when the voltage step is applied to $V_{\rm DS}$. In the case of DM, since V_{G1S} is higher than V_{G2S} after the application of the voltage step, electrons are rapidly transferred from the low-μ to the high-μ channel. Thus, the evolution of the drain current I_D, which is given by the velocity-modulation effect, is just a transient of about 0.2–0.3 ps [Fig. 5(b)], which is much shorter than that in CM. The characteristic time here is that necessary for traveling the very short distance between the high-μ and low-μ channels (40 nm) and for the adaptation of the electron velocity to the properties of the other channel (different scattering rates), as predicted in [8]. However, the huge values of $I_{\rm dis}$ appearing when the voltage step is applied in DM play a very important role in the dynamic behavior of the device. Particularly, the values taken by the gate currents just after applying $\Delta V_{\rm GDIFF} = 0.2$ V (with a time step of 1 fs) are $I_{\rm dis\_G1} = -I_{\rm dis\_G2} \sim 33300$ mA/mm since the involved geometrical input capacitance is quite high, which is of about $C_{\rm IN\_geom} \sim 167$ fF/mm, mainly due to the contribution of the intergate capacitance. In contrast, in CM, the geometrical capacitance (addition of gate–source and gate–drain capacitances) is about $C_{\rm IN\_geom} \sim 28$ fF/mm, thus leading to $I_{\rm dis\_G1} = I_{\rm dis\_G2} \sim 1400$ mA/mm, which is much lower than that in DM.

Fig. 6 presents (a) $C_{\rm gs}$ and $C_{\rm gd}$ in CM, and (b) $C_{\rm IN}$ and $C_{\rm gd}$ for the VMT operating in DM, as a function of $V_{\rm GOFF}$ for $V_{\rm DS} = 0.5$ V and $V_{\rm GDIFF} = 0$ V. The open symbols

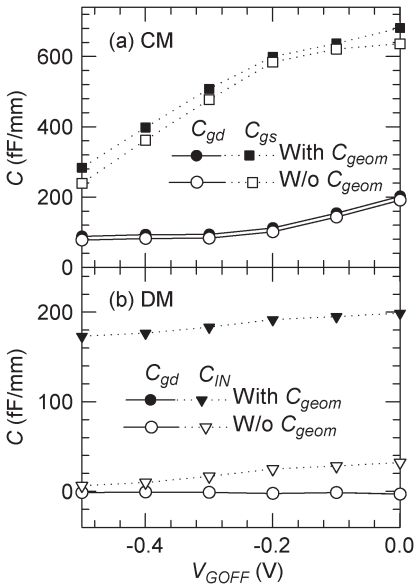

Fig. 6. $C_{\rm IN}$ and $C_{\rm gd}$ versus $V_{\rm GOFF}$ for the VMT operating in (a) CM and (b) DM, for $V_{\rm DS} = 0.5$ V and $V_{\rm GDIFF} = 0$ V. Open symbols correspond to the case in which $C_{\rm IN\_geom}$ is not considered in the calculations.

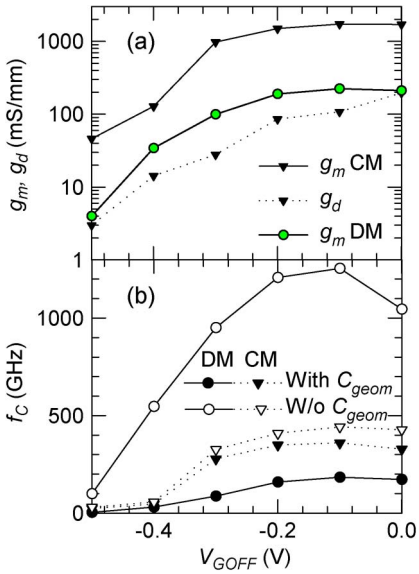

Fig. 7. (a) g_m and g_d, and (b) f_C versus $V_{\rm GOFF}$ for the VMT operating in CM and DM for $V_{\rm DS} = 0.5$ V and $V_{\rm GDIFF} = 0$ V. Open symbols correspond to the case in which the displacement currents are not considered in the calculations.

correspond to the case in which only $I_{\rm con}$ is considered in the calculation of the drain and gate currents, and therefore, the different geometrical capacitances are disregarded. When operating in CM, the values taken by $C_{\rm gs}$ and $C_{\rm gd}$ are comparable to those found in the standard DG-HEMT [5], and they are barely influenced by $C_{\rm gs\_geom}$ and $C_{\rm gd\_geom}$ since these are very small (10 and 44 fF/mm, respectively). In DM, the contribution of $C_{\rm IN\_geom}$ to $C_{\rm IN}$ is very important, i.e., 167 fF/mm, which is much higher than that coming from the channel charging/discharging $(C_{\rm gs})$, whose maximum value is about 30 fF/mm, since the electron concentration under the gates hardly changes. On the other hand, and for the same reason, $C_{\rm gd}$ is nearly zero (being the same for both cases with and without $I_{\rm dis}$).

Fig. 7(a) shows the transconductance g_m and the drain conductance g_d, and Fig. 7(b) shows the cutoff frequency f_C (which is calculated as $g_m/2\pi C_{\rm IN}$) for the VMT operating in both DM and CM as a function of $V_{\rm GOFF}$. The maximum value of g_m in DM is quite low, i.e., 224 mS/mm, compared to the CM value, which is 1724 mS/mm. The DM g_m can be improved by enhancing the difference between the mobility of the channels, e.g., by increasing the compensated doping in the low-μ channel, with the main limit being the epitaxial technology. Evidently, the values of g_d are the same in DM and CM. Remarkably, even if a much better frequency performance was expected in DM operation, the values of the intrinsic cutoff frequency of the device shown in Fig. 7(b) are much higher in CM, i.e., 359 GHz, than in DM, i.e., 184 GHz, when the total capacitances are taken into account. As advanced in Section II, the intergate capacitance C_{g1g2} (which is the main contribution to $C_{\rm IN\_geom}$ in DM) is responsible for the deficient dynamic behavior in DM, as confirmed by the excellent values (in excess of 1 THz) obtained if this geometrical contribution is disregarded. Therefore, even if the VMT offers the possibility of removing the transit-time limitation, the capacitance between

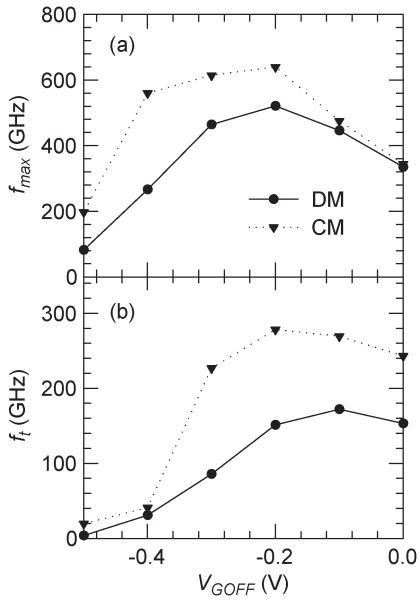

Fig. 8. (a) $f_{\rm max}$ and (b) f_t versus $V_{\rm GOFF}$ for the VMT operating in DM and CM for $V_{\rm DS} = 0.5$ V and $V_{\rm GDIFF} = 0$ V.

both gate electrodes C_{g1g2} deteriorates the global dynamic response of the device. It is worth noting that the excellent frequency performance predicted in [8] for the VMT operating in DM was done without considering the influence of C_{g1g2}.

In order to complete the study of the dynamic behavior of the VMT, the values of the extrinsic cutoff frequencies (a) $f_{\rm max}$ and (b) f_t corresponding to DM and CM operation are presented in Fig. 8 as a function of $V_{\rm GOFF}$. For their calculation, the extrinsic contact resistances have been considered. As expected from the values of f_C [Fig. 7(b)], the maximum values of f_t and $f_{\rm max}$ are significantly degraded when operating as VMT, taking values of around 172 and 521 GHz, respectively, with respect to the CM operation (working as a standard DG-HEMT), with f_t

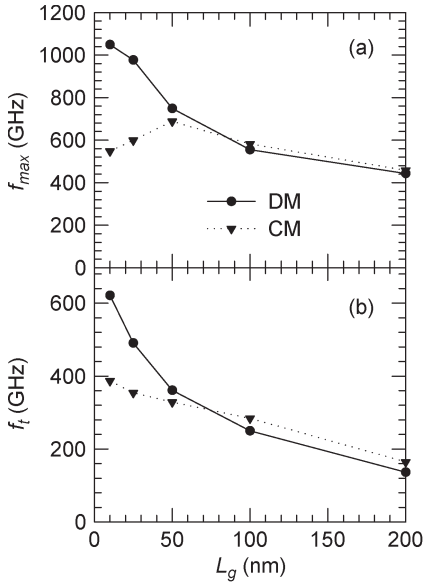

Fig. 9. Maximum values of (a) $f_{\max}$ and (b) f_t versus L_g for an optimized VMT (with compensated doping in the low-μ channel of $N_A = N_D = 5 \times 10^{18}$ cm^{-3}) operating in DM and CM, for $V_{\rm DS} = 0.5$ V and $V_{\rm GDIFF} = 0$ V.

and $f_{\max}$ of around 278 and 639 GHz, respectively. However, as already pointed out in [11], simulations of optimized VMTs reveal a significant improvement in the maximum values of $f_{\max}$ when operating in DM. For that sake, one must focus not only on the increase in g_m by increasing the difference in the velocity of electrons between the low-μ and high-μ channels but mainly on the reduction in $C_{\rm IN}$. To achieve this, the distance between the gate electrodes must be increased, having, as a limit, the reduction in g_m (i.e., the progressive suppression of the VM effect). However, the most appropriate way to reduce $C_{\rm IN}$ is shortening the gate length L_g since it does not lead to a reduction in g_m. The limit for this improvement is technological since it is very difficult to achieve a perfect alignment of both gates. Fig. 9 shows the dependence of the maximum values of f_t and $f_{\max}$ on L_g obtained in structures where the compensated doping in the low-μ channel is increased to $N_A = N_D = 5 \times 10^{18}$ cm^{-3} (the low-electric field mobility at room temperature being ~ 840 cm^2/V $\cdot$ s), so that the maximum g_m is about 320 mS/mm. In the simulated structures, just L_g has been changed, without adequately scaling the device in the vertical direction. Fig. 9 indicates that, when operating in CM, $f_{\max}$ decreases when L_g is shortened below 50 nm, whereas f_t hardly increases. However, when working in DM, both $f_{\max}$ and f_t are significantly improved when shortening L_g, thus revealing different scaling rules than in the case of standard FETs. We remark that only the intrinsic capacitances have been considered for these calculations, with no offset contribution [16], [17], so that the values presented in Fig. 9 should be considered as ideal (with no influence of crosstalk or fringing capacitances associated to the actual layout of the device electrodes).

IV. Conclusion

In this paper, we have analyzed, by means of a 2-D ensemble MC simulator, an InAlAs/InGaAs 100-nm-gate VMT based on a DG-HEMT topology. By changing the gate voltages in DM, electrons are shifted between two channels with significantly different mobilities. The MC analysis of the steady-state values of electron density and mean velocity in DM operation confirms the velocity-modulation effect appearing in the VMT. However, the dynamic behavior of the VMT is demonstrated not to be as exceptional as expected from the avoidance of channel charging/discharging due to not only the low values of g_m but also the high value of the capacitance between both gates C_{g1g2}.

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