Cryogenic Performance of Low-Noise InP HEMTs: A Monte Carlo Study

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***Abstract*— In this paper, we present a study of the cryogenic performance of InP high electron mobility transistors (HEMTs) in the low-noise region by means of Monte Carlo simulations. A decrease of the contact resistances and an increase in the electron velocity in the channel together with enhanced channel electron confinement upon cooling of the device are observed, and considered to be the reason for the excellent low-noise behavior of cryogenic InP HEMTs. These findings are supported by a good agreement between simulated and experimental DC, RF, and noise figure data of a 130-nm gate length InP HEMT at 300 and 77 K. An increase of the transconductance g_m and gate-to-source capacitance C_{gs} is observed when cooling from 300 to 77 K as a consequence of electron velocity increase and improved channel confinement.**

***Index Terms*— Cryogenic temperature, InGaAs/InAlAs/InP high electron mobility transistor (HEMT), low noise, Monte Carlo simulations, noise parameters.**

I. Introduction

DUE TO its very low-noise figure at cryogenic temperatures, InGaAs/InAlAs/InP high electron mobility transistors (HEMTs) are considered the best transistors for cryogenic low-noise amplifiers (LNAs). Despite being a relatively established technology, only a few studies are reported about the physical understanding of the improved noise performance of InP HEMTs at cryogenic temperatures between 10 and 100 K [1], [2]. The understanding of the low temperature behavior of these devices in the low-bias region is critical for the low-noise optimization at cryogenic temperatures. Indeed, it is known that optimizing noise figure for the InP HEMT at room temperature does not necessarily mean that the noise figure is optimized under cryogenic conditions [1].

In this paper, a complete study of the cryogenic performance of InP HEMTs in the low-noise region is presented. We have taken advantage of Monte Carlo (MC) simulations for the understanding of the low-temperature performance of the devices, and have validated our simulation method by comparison with the experimental data. MC simulations have demonstrated as a powerful technique for the simulation of InGaAs HEMTs [2]–[6]. As MC simulations are performed in the time domain, they can provide accurate noise results. This, together with the fact that MC can account for the ballistic transport, common in these devices due to the high mobility of the channel, makes MC the most appropriate simulation technique for studying low-noise properties of InP HEMTs. Furthermore, MC simulations provide a valuable insight into the electron transport at low temperature within the device, allowing increased understanding of the experimental results.

In this paper, DC, RF, and noise performance have been studied by means of MC simulations and compared with the experimental results at 300 and 77 K. A special focus is made on the low-current regime below 300 mA/mm, where the InP HEMT is normally operated under low-noise conditions.

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II. Simulation Model

The experimental device is a 2×10 μm InP HEMT. We can safely perform 2-D simulations and assume that the device is homogenous in the third dimension. A 2-D MC simulator, self-consistently coupled with a Poisson solver, has been used for the simulations [6]–[8]. This model has previously been shown to be a powerful method for the simulation of InP HEMTs at 300 K [7]. In this paper, the simulator has been used to simulate cryogenic temperatures down to 77 K.

The conventional operating temperature of cryogenic LNAs is 4–15 K. In this paper, 77 K has been used as the device cryogenic temperature. In general, the DC and RF experimental behaviors of the cryogenic InP are similar at 77 K (this paper) and at 10 K [9]. The semiclassical simulation approach used in this paper behaves well at 77 K but is much less reliable at 10 K due to quantum effects. Strictly speaking, a multi-sub-band transport approach would be necessary, considering the electron transport to be quasi-2-D (considering the intra-sub-band and inter-sub-band scattering processes). This precise description of transport would excessively increase the computation load. In our simulations, we have chosen to use a simple approach in which some quantum effects are roughly taken into account, as explained in [6]. This model allows us to correctly reproduce the effective electron mobility and the concentration distribution in the channel, which are the main parameters that determine the HEMT performance. Indeed, when applying high drain voltages, the electron heating erases

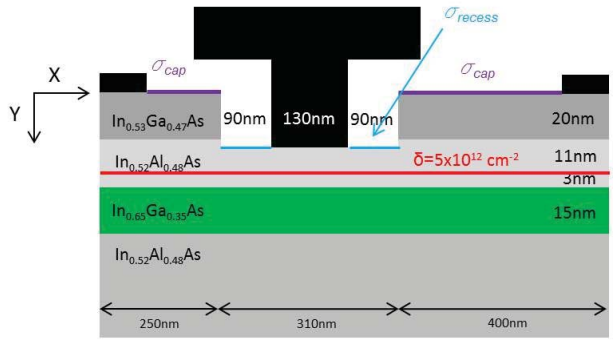

Fig. 1. Schematic of the simulated InP HEMT.

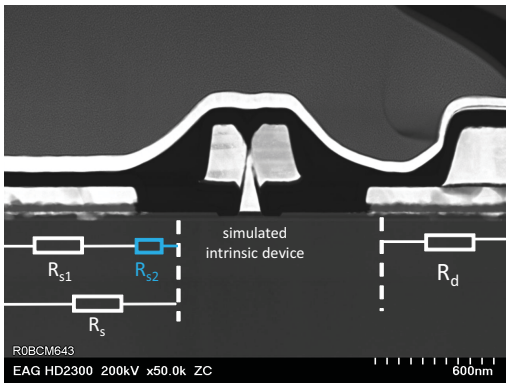

Fig. 2. Scanning transmission electron microscopy image of the fabricated InP HEMT. The intrinsic simulated area and external resistances are indicated.

part of the quantum effect, since most of the carriers are not confined to the lower energy sub-bands. The higher is the applied electric field, the less influence of quantum effects on the InP HEMT simulations [10].

The device under study is a 130-nm gate length InP HEMT specifically optimized for low-noise operation under cryogenic conditions [11]. The device topology needed for the simulations was provided by cross-sectional micrographs of fabricated HEMTs. A schematic of the simulated device can be seen in Fig. 1. The depth and length of the recess were 23 and 90 nm, respectively. The epitaxial structure was based on an InP substrate, followed by a 500-nm $In_{0.52}Al_{0.48}As$ buffer, a 15-nm $In_{0.65}Ga_{0.35}As$ channel, and a 13-nm $In_{0.52}Al_{0.48}As$ barrier. The 20-nm-thick $In_{0.53}Ga_{0.47}As$ cap layer was heavily doped (5×10^{19} cm^{-3}) in order to improve the ohmic contacts. Electrons were introduced in the channel by a planar Si δ-doping of 5×10^{12} cm^{-2}. Ge-based alloyed ohmic contacts were fabricated. The fabrication process has been described in [11].

In order to reduce the simulation time, the ohmic source–recess region was shortened from the experimental value of around 400 to 250 nm. The omitted part can be introduced as a contribution to the external source resistance [6] R_{s2} (Fig. 2).

In the experimental epitaxial structure, the cap layer was heavily doped, which resulted in extended simulation times. As the effect in the intrinsic device of the dopant level of the cap layer was almost negligible, the doping level was decreased to 5×10^{18} cm^{-3}, and the external resistances were adjusted accordingly.

TABLE I
EXTRACTED EXPERIMENTAL VALUES FOR THE PARASITICS OF 2×10 μm InP HEMT AT 300 AND 77 K. UNITS ARE fF, pH, AND Ω

Parasitics	300 K	77 K
C_{pg}, C_{pd}	18	22
L_g	46	36
L_s	3	5
L_d	22	63
R_g	0.5	0.25

To reproduce the surface charges appearing in the semiconductor–passivation interface, a simple constant surface charge model was considered in the simulations. A negative surface charge density σ_{cap} was considered in the top of the cap layer (Fig. 1). The negative surface charge at the recess floor σ_{recess} depends on the recess etching process and may differ from the one at the top of the cap layer [6]. σ_{cap} and σ_{recess} were adjusted in order to reproduce the experimental Hall sheet electron density in the channel n_s at 300 and 77 K. The temperature dependence of n_s was extracted from Hall data measured from 300 to 10 K on Van der Pauw structures fabricated with the same recess etch, process, and epitaxial structure as the InP HEMT.

An experimental n_s of 1.4×10^{12} cm^{-2}, independent of temperature, was extracted. The values of σ_{cap} and σ_{recess} which satisfied the experimental n_s were $\sigma_{cap}/e = -5 \times 10^{12}$ cm^{-2} and $\sigma_{recess}/e = -2.2 \times 10^{12}$ cm^{-2}. The electron mobility of the structure was 12 000 cm^2/Vs and 56 000 cm^2/Vs at 300 and 77 K, respectively.

The gate leakage current I_G was not incorporated in the simulation model. The experimental InP HEMTs studied here displayed very low I_G (200 nA/mm [300 K] and 20 nA/mm [10 K] [9]) at the bias conditions studied here. As a result, the effect from the gate leakage on device noise behavior was considered negligible [12].

The Schottky barrier height V_{Sch} was introduced externally in the MC simulations. We considered values of V_{Sch} of 0.35 and 0.38 V, respectively at 300 K and 77 K. These values of V_{Sch} were obtained by comparing the threshold voltage obtained with MC with the experimental value.

In order to compare the intrinsic MC results with the extrinsic experimental data for the studied 2×10 μm HEMTs, the effect of the parasitics must be included (for details, see [7]). Experimental values of the extrinsic parameters were added to the intrinsic experimental results (Table I). The extracted values of L_g and L_d resulted to be very sensitive to the position of the probes leading to a large uncertainty. However, the inaccuracy of these values had no influence in this paper. In the case of source resistance R_s and drain resistance R_d, one cannot simply introduce experimental contact resistances as we have to account for R_{s2} and for the decrease of the dopant level of the cap layer. The values of R_s and R_d were determined by DC comparison between extrinsic experimental results and intrinsic MC ones. Values of $R_s = 0.1$ Ω mm and $R_d = 0.06$ Ω mm were considered in the simulations at 300 K, and $R_s = 0.05$ Ω mm and $R_d = 0.03$ Ω mm at 77 K, slightly lower than the experimental values. Upon cooling from

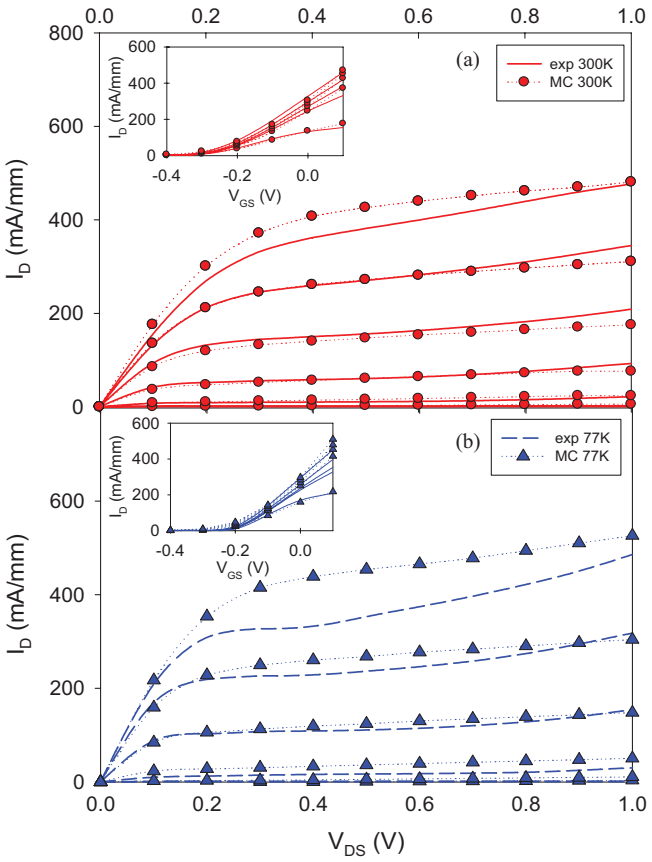

Fig. 3. I_D versus V_{DS} for $V_{GS} = -0.4$ to 0.1 V with a step of 0.1 V. Simulated results (dotted lines with symbols) versus experimental data (lines) (a) for 300 K and (b) for 77 K. Insets: simulated and experimental I_D versus V_{GS} for V_{DS} from 0.1 to 0.9 V with step 0.2 V (a) at 300 K and (b) at 77 K.

300 to 77 K, simulated parasitic source and drain resistances had to be halved, to be in good agreement with the experimental results (around 0.25 Ω mm at 300 K and 0.12 Ω mm at 10 K [9]).

Simulated small signal equivalent circuit (SSEC) parameters were obtained from the admittance parameters obtained by Fourier analysis of the response of the transistor currents to voltage steps applied at the gate and drain contacts [7]. For a correct comparison between the intrinsic experimental and simulated equivalent circuits, we had to consider that even when de-embedding the extrinsic parameters from the experimental results, there were still effects that the MC was not accounting for, such as fringing and crosstalk capacitances in the layout [7]. As a result, three extrinsic capacitances C_{gs}^{extr}, C_{gd}^{extr}, and C_{ds}^{extr} were added to the MC results to reproduce the effects associated with the topology of the devices. These capacitive elements were obtained from comparison with the experimental results at drain current $I_D = 0$ [7].

III. DC Characterization

In Fig. 3, the experimental and simulation results of I_D versus drain voltage V_{DS} at 300 and 77 K are compared. A good agreement between the experimental results and MC is observed for the low-current region (below 300 mA/mm). For gate voltage V_{GS}=−0.3 V and higher, the experimental

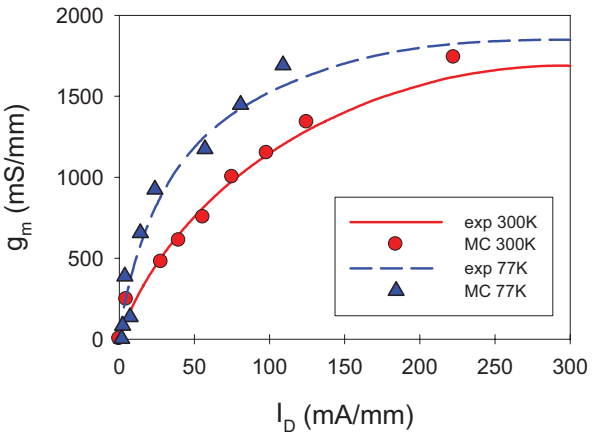

Fig. 4. Comparison of the experimental transconductance (lines) and the MC ones (symbols) versus I_D at 300 K (red solid line, red circles) and 77 K (blue dashed line, blue triangles), both for $V_{DS} = 0.6$ V.

measurements exhibit a kink effect which becomes more pronounced at 77 K. The kink is not related to impact ionization as it appears for a relatively low value of V_{DS} (around 0.4 V). We attribute the kink in Fig. 3 to the presence of traps at the bottom of the recess [13] whose effect increased when cooling to 77 K [14]. This mechanism was not included in the simulations, and therefore, the kink was not observed in the MC results. This paper focuses on the low-noise regime of the InP HEMT, or equivalently, I_D below 300 mA/mm. This region is not affected by the kink behavior. Here, a good agreement between the experimental data and MC is observed in Fig. 3 for both 300 and 77 K. For current higher than 300 mA/mm, the disagreement between MC simulations and experimental results increases. This is due not to a poor description of the electron transport but to the lack of a precise description of the bias dependence of the surface charges not included in the MC model. This model provides a good description of the low-current region, since these are the bias conditions used for low-noise applications, even if some discrepancies are found for higher gate voltages.

The inset of Fig. 3 shows the simulation results and experimental data for I_D versus V_{GS} at 300 and 77 K. A shift in the threshold voltage of around 0.1 V is observed when cooling down.

IV. Microwave Characterization

The SSEC transconductance g_m, gate–source capacitance C_{gs}, and gate-drain capacitance C_{gd}, were compared at 300 and 77 K at $V_{DS} = 0.6$ V for MC simulations and experimental results.

Experimentally, a large increase of g_m was observed in the low-current region when reducing temperature from 300 to 77 K (Fig. 4). For $I_D = 50$ mA/mm, g_m reached a value of 1200 mS/mm at 77 K, whereas at 300 K, g_m was 750 mS/mm. A good agreement was observed between experimental and simulation results at both 300 and 77 K, and the simulations reproduced the experimental increase of g_m at 77 K.

Fig. 5 shows a comparison between the experimental results and MC for C_{gs} at 300 and 77 K. C_{gs}^{extr} was included in the simulations with values of 360 fF/mm for 300 K, and

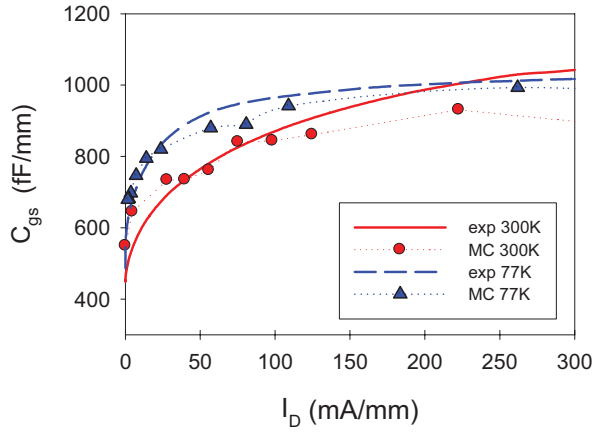

Fig. 5. Comparison of the experimental data (lines) and the MC results (symbols, dotted lines) for C_{gs} versus I_D at 300 K (red solid line, red circles) and 77 K (blue dashed line, blue triangles), all for $V_{DS} = 0.6$ V.

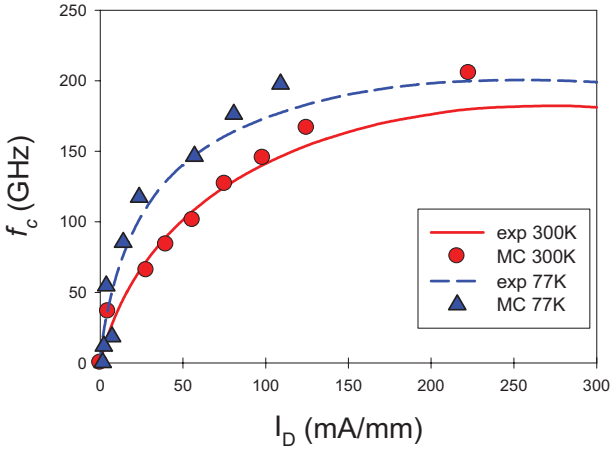

Fig. 6. f_c obtained from the experimental (lines) and from the MC (symbols) SSEC parameters as a function of I_D at 300 K (solid red line, circles) and at 77 K (dashed blue line, triangles), all for $V_{DS} = 0.6$ V.

450 fF/mm for 77 K. These capacitances are in the same order as reported in previous works [7]. C_{gs} increases in the very low-current region when cooling down from 770 fF/mm at 300 K to 910 fF/mm at 77 K at $I_D = 50$ mA/mm. In contrast, simulated and experimental values of C_{gd} (not shown) are more or less constant and are not affected by cooling to 77 K.

An estimation of the intrinsic cut-off frequency f_c obtained from the SSEC parameters through equation $f_c = g_m/2\pi(C_{gs} + C_{gd})$ is plotted in Fig. 6. f_c increases at 77 K which is due to the increase of g_m upon cooling.

The simulated extrinsic cut-off frequency f_T was obtained from the simulated current gain $|H_{fe}|^2$ by using the frequency-dependent Y-parameters extracted from the MC simulations, that is, not using the equivalent circuit approach [8]. As can be observed in the inset of Fig. 7, simulated $|H_{fe}|^2$ shows the expected 20-dB/dec decay up to 50 GHz. For frequencies above 50 GHz, the low-frequency equivalent circuit is not valid any more as the parameters become frequency dependent [8]. The simulated result of f_T was obtained by the extrapolated value of the low frequency 20-dB/dec decay.

Fig. 7 shows a good agreement between the simulation results for f_T at 300 and 77 K and the experimental measurements in the current range under study. The discrepancies

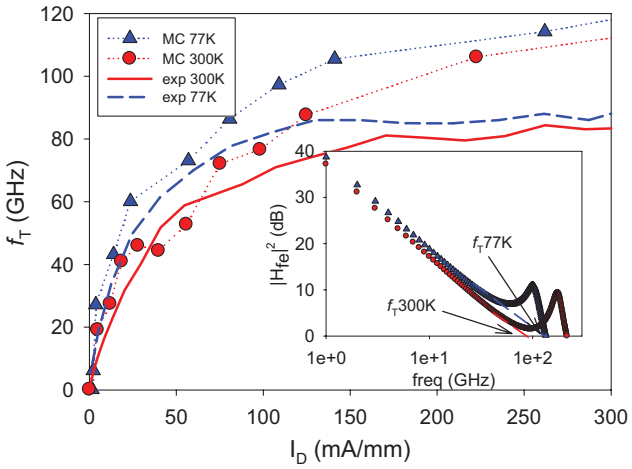

Fig. 7. Simulated (symbols, dotted lines) and experimental (lines) f_T versus I_D at 300 K (red circles, red solid line) and 77 K (blue triangles, blue dashed line) for $V_{DS} = 0.6$ V. Inset: simulated $|H_{fe}|^2$ versus frequency at 300 K (red circles) and 77 K (blue triangles). Extrapolated f_T is marked.

between the simulation and the experimental values increase for high current levels (also observed in Fig. 6) due to the presence of the kink, which is not well described by our simple surface charge model. A moderate increase of f_T can be observed when decreasing the temperature (around 20 GHz for $I_D = 100$ mA/mm).

V. Noise Performance

The very low noise level of the InP HEMT makes it impossible to perform direct noise measurements. The extraction of experimental noise parameters has to be therefore performed indirectly by measuring the noise figure from an LNA design based on the studied transistors [11]. In this paper, we have used the MC simulations to compare the intrinsic and extrinsic noise of the InP HEMT at 300 and 77 K.

Intrinsic noise properties were analyzed using the P, R, and C noise parameters [15], [16]. For a proper comparison of the 300 and 77 K results, P, R, and C have been defined as

$$P = \frac{S_{i_d}}{4K_B T_0 |Y_{21}|}, \quad R = \frac{S_{i_g} |Y_{21}|}{4K_B T_0 |Y_{11}|^2}, \quad jC = \frac{S_{i_g i_d}}{\sqrt{S_{i_g} S_{i_d}}} \quad (1)$$

where T_o is the reference temperature of 290 K; and Y_{11}, Y_{12}, Y_{21}, and Y_{22} are the admittance parameters of the intrinsic device. S_{id}, S_{ig}, and S_{igid} are the spectral densities of the drain current, gate current, and their cross-correlation, respectively. P represents the normalized channel noise due to fluctuations in the carrier velocity, R the gate noise due to charge fluctuations in the channel, and C the correlation between them. Note that the simulated values of R and C are not very precise due to the uncertainty in the MC simulation of the gate current fluctuations [7].

In Fig. 8, we present intrinsic values of the three intrinsic noise parameters as a function of current for 300 and 77 K. The results at 300 K agree well with previous results of noise in similar InP HEMTs using MC simulations [7]. The improvement in the intrinsic noise upon cooling is not very high; however, a decrease of P and R, as well as an increase in C is observed when comparing the 300 and 77 K results.

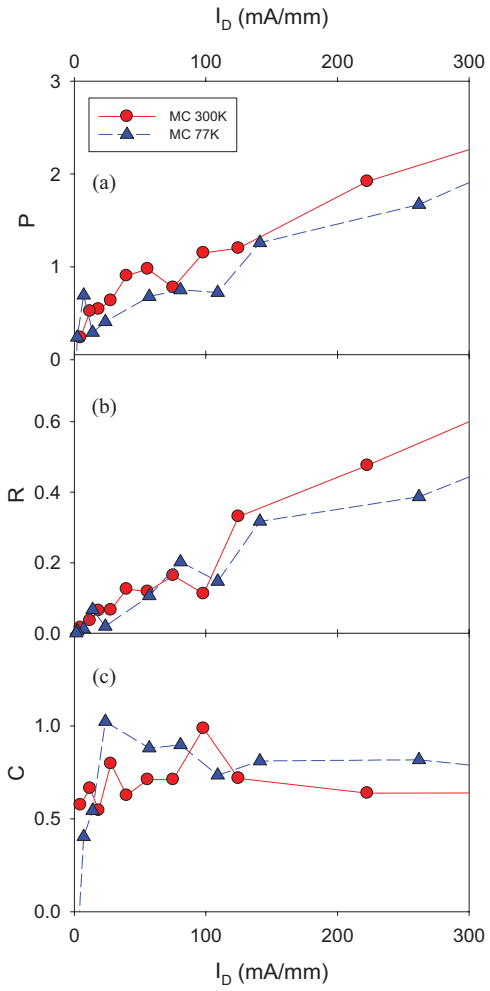

Fig. 8. Simulated intrinsic noise parameters (a) P, (b) R, and (c) C as a function of the drain current at 300 K (red circles, solid red lines) and 77 K (blue triangles, dashed blue lines). All simulations are done at $V_{DS} = 0.6$ V.

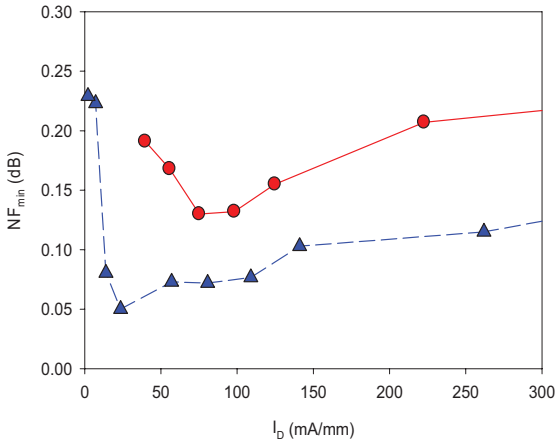

Fig. 9. Simulated minimum noise figure as a function of the drain current at 300 K (red circles, red solid line) and 77 K (blue triangles, blue dashed line) for 6 GHz at $V_{DS} = 0.6$ V.

All of these variations contribute in the right direction for the reduction in the noise figure.

The extrinsic minimum noise figure NF_{min} was obtained from MC simulations at 300 and 77 K at 6 GHz and $V_{DS} = 0.6$ V, which included the influence from the extrinsic

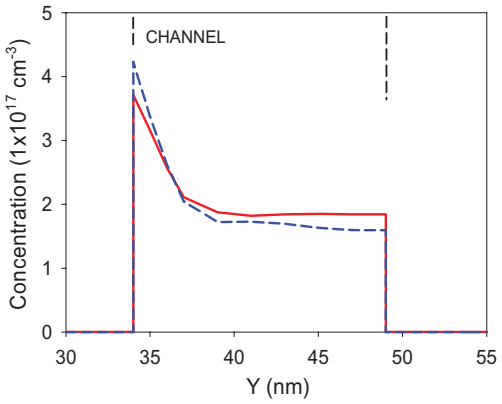

Fig. 10. MC simulated electron concentration profile under the gate along the Y-direction at 300 K (red continuous line) and at 77 K (blue dashed line) for $V_{DS} = 0.6$ V and $I_D = 250$ mA/mm.

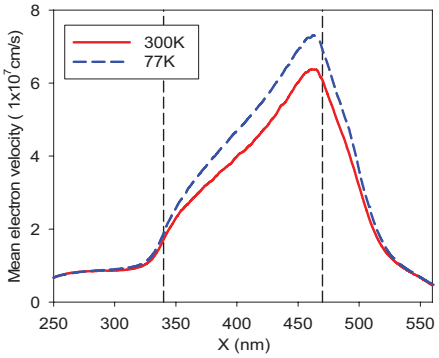

Fig. 11. MC mean electron velocity profile along the channel under the gate at 300 K (red continuous line) and at 77 K (blue dashed line) for $V_{DS} = 0.6$ V and $I_D = 250$ mA/mm. Drain is at the right side, source to the left.

elements of the SSEC [17]. Fig. 9 shows a comparison of NF_{min} at 300 and 77 K. A minimum in the simulated NF_{min} of 0.15 dB is observed around 80 mA/mm for 300 K, and 0.05 dB at 20 mA/mm for 77 K. From the experimental measurements of a 4- to 8-GHz LNA based on 2×100 μm InP HEMTs (fabricated in the same batch as the 2×10 μm studied InP HEMT in this paper), a minimum in the noise figure was observed at $I_D = 75$ mA/mm for 300 K and at $I_D = 15$ mA/mm for 10 K [9]. This suggests that the MC simulations capture the behavior of the experimental NF_{min} versus I_D.

VI. Discussion

The effect of the microscopic electron transport on the cryogenic performance of InP HEMTs has been studied taking advantage of the MC simulations. In Fig. 10, the transversal profiles of electron concentration under the gate at 300 and 77 K are compared at $V_{DS} = 0.6$ V and $I_D = 250$ mA/mm. Confirming previous suggestions in [9], more electrons are located in the upper part of the channel at 77 K than for 300 K. Qualitatively, 1-D Schrödinger–Poisson results (not shown here) confirmed this MC result. This improvement of the 2-D electron gas (2-DEG) confinement at low temperature is a consequence of the thermal energy decrease of the electrons and implies a better gate control. This improved gate control under cooled conditions for the InP HEMT has several

important consequences for the device DC characteristics: an increase of the slope in g_m, an increase of C_{gs} in the low-current region, and a shift in the threshold voltage.

Fig. 11 shows the mean electron velocity of the electrons along the channel under the gate region at 300 and 77 K. At both temperatures, the velocity peaks at the drain side of the gate where the electric field is at maximum. The expected [2] increase in the mean electron velocity upon cooling (around 17% at $x = 470$ nm in Fig. 11), leads to the observed increase of the transconductance (Fig. 4).

Physically, the increase in mean electron velocity with reduced device temperature, observed in Fig. 11, is due to the reduction of the scattering rates leading to an increase of the mean electron free path.

A significant improvement in NF_{min} was obtained upon device cooling. Two contributions can be distinguished in the noise reduction, one from the decrease of the contact and access resistances with temperature, the other from the lower intrinsic noise in the device. The latter also leads to a shift of the minimum NF_{min} toward lower I_D.

VII. Conclusion

A study of the cryogenic performance of a 130-nm gate InP HEMT by MC simulations was presented. Simulated DC and RF results were compared with the experimental data, proving an excellent agreement at low $I_D < 300$ mA/mm, which validated the simulation model. An increase not only in (intrinsic) g_m but also in C_{gs} was observed experimentally when cooling from 300 to 77 K. This observation was in agreement with an improvement in the 2-DEG channel confinement together with an increase of the mean electron velocity under the gate. An increase of around 20% was observed upon cooling from 300 to 77 K in f_T at 100 mA/mm, in both simulated and experimental data. Regarding the device noise behavior, the intrinsic P, R, and C parameters revealed a slight decrease at 77 K, whereas a significant decrease in NF_{min} was observed. The total noise improvement comes not only from a better intrinsic behavior (including a shift to lower I_D of the optimum noise conditions) but also from a decrease of the resistance of the contacts and access regions. A simulated minimum of NF_{min} of 0.13 dB at 6 GHz was obtained at 80 mA/mm for 300 K, and 0.05 dB at 20 mA/mm for 77 K.

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