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Numerical and experimental study of a 0.25 μm fully-depleted silicon-on-insulator MOSFET: static and dynamic radio-frequency behaviour

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Abstract

We investigate the static and dynamic characteristics of a 0.25 μm gate-length fully-depleted silicon-on-insulator metal–oxide–semiconductor field effect transistor. Considering properly the physical topology of the transistor with its accesses, numerical simulations are performed using a two-dimensional ensemble Monte Carlo simulator and these are compared with experimental results. Moreover, in the simulation we include important effects that appear in real transistors, such as surface charges, contact resistances, impact ionization phenomena and extrinsic parasitic capacitances. The appearance of a velocity overshoot region near the drain, together with the presence of hot carriers in the channel, is observed in the saturation regime. The dynamic behaviour of the device is described through significant small signal equivalent circuit parameters, which are examined by means of internal quantities (such as profiles of the internal electron concentration), provided by numerical simulations. In general, the device shows excellent performance in terms of important design parameters, such as transconductance-to-current ratio, transconductance and cut-off frequency together with a reduced capacitive coupling to the substrate. The results of the Monte Carlo simulations show an exceptional agreement with the experimental data, thus confirming the validity of the simulator as a reliable tool for the analysis of the influence of geometrical and electrical parameters on the static and dynamic performance of the device.

1. Introduction

The enormous advance in mobile communications achieved in the last few years has made it necessary to develop radio-frequency (rf) front-ends at a low cost with the lowest level of noise. When the reduced cost is a major concern, silicon-based technologies seem to be the most adequate to accomplish this objective. With this purpose, many efforts have been made to advance the progressive reduction of the dimensions of bulk silicon metal–oxide–semiconductor field effect transistors (MOSFETs) [1]. Nevertheless, although rf CMOS circuits have been already demonstrated [2], and they are undoubtedly a promising technology, the shrinkage in bulk device geometries to the deep-submicrometre scale presents

many technological problems [1], mainly due to strong short channel effects. At this point, when bulk devices begin to face significant limitations, silicon-on-insulator (SOI) technology becomes a key solution [3].

Although the SOI idea is not new at all, the possibilities of SOI MOSFETs have been fully explored only in these last few years thanks to the advances in the fabrication process. Especially in the case of fully-depleted (FD) SOI MOSFETs, many advantages can be seen over traditional bulk devices [3, 4]: the absence of latch-up, higher soft-error immunity, shorter and easier CMOS processing, sharper subthreshold slope, and reduced electric fields, parasitic capacitances, and short-channel effects together with a higher transconductance and lower threshold voltage. As a consequence, a very good high-frequency performance is obtained and the devices may operate at lower voltages, thus reducing the power consumption. Furthermore, front-end processing is cheaper in SOI than in bulk CMOS, and a higher packing density is also achieved [3].

For these many reasons, FD SOI technology has attracted extraordinary interest in recent years, and it can be affirmed that it has fully joined the microelectronics roadmap. Therefore, in order to accelerate the development of future generations of SOI devices and their applications, it has become necessary not only to accurately characterize and study the high-frequency performance, but also to obtain a good comprehension of the inner physics of these devices. To reach this goal, the aid of computer simulation is of primary importance. Traditional simulation methods, such as drift–diffusion or hydrodynamic models, present critical restrictions when applied to the study of MOSFETs with small dimensions, where short channel effects such as velocity overshoot or the appearance of hot carriers become important. The ensemble Monte Carlo (EMC) method [5] is the most adequate simulation technique to deal with this problem, since it is based on a microscopic approach and, as a consequence, it includes in a natural way the main effects associated with small devices.

The purpose of this work is to analyse the static and dynamic characteristics of 0.25 μm gate-length FD SOI n-MOSFETs. The devices studied in this paper have already been used for designing various classical analogue and digital circuits: operational transconductance amplifiers, base band circuits (a sigma-delta modulator, a rf quadrature generator, low pass filters, etc), microwave oscillators at 6 and 12 GHz [6] and a 2 GHz GSM receiver [7], showing an exceptional dynamic behaviour and one of the best noise microwave performances reported in the literature [8]. Due to the lack of simulation tools, the topology of the circuits is not fully optimized nor are the devices themselves. To investigate in depth the physical behaviour of deep sub-micrometre FD SOI devices and to draw some optimization directions for future MOSFET generations, EMC simulations are carried out. Several requirements have to be fulfilled to assure the validity of the calculations. First of all, the doping profiles and geometry (oxide thickness, length of the overlap regions, etc) of the different layers of the fabricated device under analysis must be reproduced as accurately as possible. Secondly, important real effects also have to be considered, such as surface charges or impact ionization phenomena. Finally, the extrinsic experimental parasitics, such as parasitic resistances and capacitances associated with the feed lines, should be taken into account in the EMC results to perform the comparison between simulation and experimental results. In this way, the EMC method can be reliably used to analyse both the static and dynamic behaviours of the devices, the bias dependence of small-signal equivalent circuit (SSEC) parameters and complementarily to investigate the influence of geometrical factors or surface charges, with the advantage of providing a microscopic physical interpretation in terms of quantities such as velocity, energy or concentration of carriers. Thus, once the simulator has confirmed its reliability, 'computer experiments' can be performed, and many questions raised by the experimental measurements can be addressed [9].

The paper is organized as follows. In section 2, the FD SOI structure under analysis and the main features of our EMC simulator are presented. In section 3, the experimental and simulated static characteristics are studied, including important parameters such as the transconductance-to-drain current ratio, and internal quantities such as electron concentration, velocity and energy. The dynamic response of the device is analysed in section 4, paying special attention to the SSEC capacitances. The majority of the results shown in this paper correspond to saturation bias conditions, since this is the operation region of main interest in these devices for analogue applications. Finally, the main conclusions of our work are presented.

2. Structure under analysis and Monte Carlo procedure

A CMOS-compatible process on 200 mm UNIBOND® wafers was employed for the fabrication of the FD SOI MOSFETs under analysis in this paper. The thickness of the buried oxide is 0.4 μm and the thickness of the active silicon is thinned down to 30 nm in order to ensure completely the depletion of holes in the active layer, thus eliminating floating body effects. The transistors have a gate length of 0.25 μm, and are composed of eight gate fingers in parallel of 6.25 μm and 12.5 μm each. In order to lower the contact resistances, a titanium salicide process was used. A more complete description of the device topology and fabrication process can be found in [7].

For the numerical calculations, we use a two-dimensional (2D) semi-classical bipolar EMC simulator self-consistently coupled with a Poisson solver. This method has been successfully applied to the study of several Si and SiGe devices, such as heterojunction bipolar transistors (HBTs) and bipolar junction transistors (BJTs) [10] or MOSFETs [11]. Both electron and holes are simulated as particles, which allows us to properly evaluate the influence of each type of carrier. The simulation of holes is justified by the fact that holes in the substrate may play an important role in the dynamic behaviour of the device [11], and also by the possible appearance of impact ionization phenomena in the active layer. The size of the mesh ranges from 10 to 250 Å in order to solve accurately the Poisson equation. The time step is 1 fs.

Figure 1 shows the geometry of the simulated structure. Important experimental parameters, such as overlap length

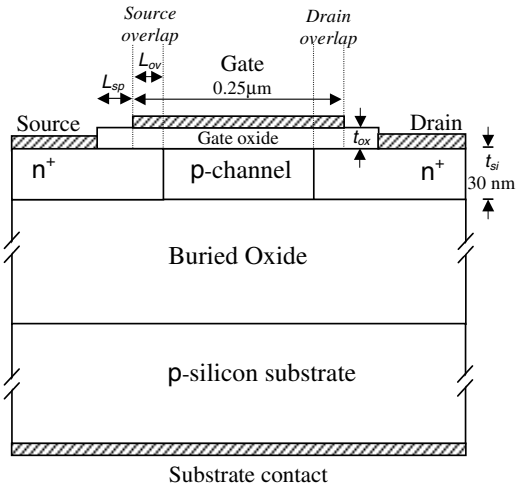

Figure 1. Schematic diagram of the simulated FD SOI device. The diagram is not scaled.

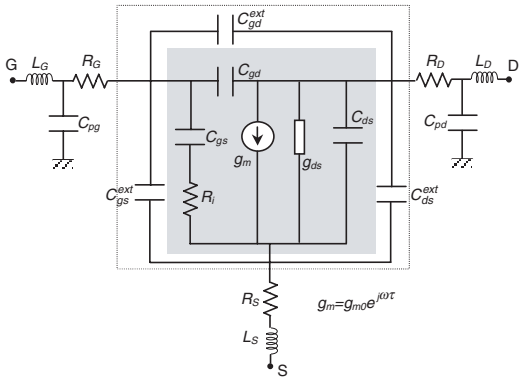

Figure 2. Small-signal equivalent circuit of the device. The shaded area represents the intrinsic elements obtained by the EMC simulation. The 'intrinsic' device from the point of view of experimental measurements is enclosed in the dotted box; this includes the effect of parasitic extrinsic capacitances and excludes contacts parasitics.

(L_{ov}), spacer oxide length (L_{sp}), oxide thickness (t_{ox}), doping profiles, etc, take their real values, in an attempt to reproduce the geometry of the fabricated devices. The device is considered to operate in common-source configuration, with source and substrate contacts short-circuited. Since our simulator is bi-dimensional, the width of the devices (W) corresponds to the non-simulated dimension. Accordingly, the majority of the results shown in this paper are properly normalized by the total width. To compare with experimental results, we focus on the devices with the largest width $W(8 \times 12.5\ \mu\text{m})$ in order to reduce the possible influence of parasitic effects associated with a short device width, such as fringing capacitances at the end of the gate fingers. Nevertheless, it has to be stressed that the comparison of the EMC calculations with the experimental results for the devices with a shorter width is very similar to that reported here for the FD SOI MOSFETs with a larger W, which indicates that no significant additional parasitic effects appear when the finger width is reduced from 12.5 μm to 6.25 μm.

The effect of external series resistances in the drain and source terminals can be taken into account by considering self-consistently the voltage drop due to these resistances [12] for each time step

$$V_{\text{GS}}^{\text{int}} = V_{\text{GS}} - R_{\text{S}} I_{\text{D}} \tag{1}$$

$$V_{\text{DS}}^{\text{int}} = V_{\text{DS}} - (R_{\text{S}} + R_{\text{D}}) I_{\text{D}} \tag{2}$$

where V_{DS} and V_{GS} are the external potentials applied in contacts, $V_{\text{DS}}^{\text{int}}$ and $V_{\text{GS}}^{\text{int}}$ are the voltages applied to the intrinsic device, R_{S} and R_{D} are the source and drain contact resistances, and I_{D} is the drain current.

Real effects appearing in the fabricated devices, such as surface charges [9] or impact ionization processes have also been taken into account. In the case of surface charges, we consider a static surface charge at the oxide–semiconductor boundaries [9]. The boundary condition for the Poisson solver at these surfaces is

$$\varepsilon_1 E_1 - \varepsilon_2 E_2 = \sigma_{12}, \tag{3}$$

where ε_i and E_i are, respectively, the permittivity and the electric field normal to the surface, whereas indexes 1 and 2 represent the oxide and the semiconductor, respectively. σ_{12} is the surface charge associated with the oxide–semiconductor interface. Different surface charges are placed in the channel, the spacer and the overlap regions, since they correspond to different materials (p-doped Si in the channel and n-doped Si in the overlap and spacer regions). The values for these charges can be adjusted (within the range given by experimental studies) in order to achieve a good fit of the EMC results to the measured current–voltage (I–V) characteristics [9]. Dirichlet conditions are applied in the four terminals, and the von Neumann condition ($E_i = 0$) is taken into account at the limits of the simulation domain. The contacts are considered to be ohmic. More details about the EMC simulator are given in [11].

For the treatment of impact ionization processes, we adopt a Kane model [13], fitting the free parameters in order to reproduce the experimental data of bulk ionization coefficients [14, 15]. The threshold energy is 1.3 eV. Interesting phenomena such as parasitic bipolar action could be analysed if necessary, since our simulator allows us to follow the dynamics of possible holes generated in the active layer.

To determine the SSEC parameters by means of an EMC simulator, the intrinsic admittance (Y) parameters must be calculated as a previous step. The Y parameters are evaluated through the Fourier analysis of the transient response of the device to voltage steps applied separately in the gate and drain contacts. The complete procedure is described in [16]. Once the Y parameters are determined, the elements of the SSEC can be calculated [17, 18].

The SSEC circuit considered in this work is shown in figure 2. The shaded area represents the intrinsic device, and corresponds to the parameters directly calculated by the EMC simulation. To represent the parasitic capacitive effects associated with the topology of the device, the extrinsic capacitances $C_{\text{gs}}^{\text{ext}}$, $C_{\text{gd}}^{\text{ext}}$ and $C_{\text{ds}}^{\text{ext}}$ (which are considered to be bias-independent) have been added to the SSEC scheme. Their values have been determined as the difference between the experimental data and the intrinsic EMC results at zero

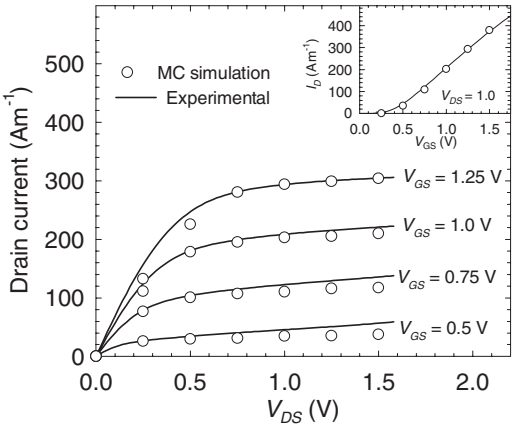

Figure 3. Drain current as a function of drain-to-source voltage for V_{GS} ranging from 0.5 to 1.25 V. The inset shows the transfer characteristic for a drain voltage of 1.0 V.

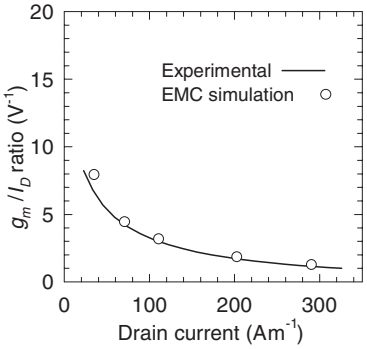

Figure 4. The ratio $g_{\mathrm{m}}/I_{\mathrm{D}}$ as a function of I_{D}.

current, where only the effect of geometric capacitances, both intrinsic and extrinsic, remains. For the FD SOI MOSFET device under analysis, these values were found to be $C_{\mathrm{gs}}^{\mathrm{ext}} = 214$ fF mm^{-1}, $C_{\mathrm{gd}}^{\mathrm{ext}} = 126$ fF mm^{-1}, and $C_{\mathrm{ds}}^{\mathrm{ext}} \approx 0$ fF mm^{-1}. Since these parasitic effects cannot be directly simulated in a 2D model, we must add these capacitances to the EMC results in a post-processing stage [9] in order to enable a direct comparison between EMC results and experimental data. The dotted box in figure 2 encloses the 'intrinsic' equivalent circuit from the point of view of experimental measurements, which includes $C_{\mathrm{gs}}^{\mathrm{ext}}$, $C_{\mathrm{gd}}^{\mathrm{ext}}$ and $C_{\mathrm{ds}}^{\mathrm{ext}}$, and excludes the effect of contact resistances, capacitances and inductances [19]. Therefore, the Y parameters directly obtained by the MC method $\left(Y_{ij}^{\mathrm{MC}}\right)$ are modified by means of the following relationships [9] to provide the final intrinsic Y parameters (Y_{ij}):

$$\begin{aligned} Y_{11} &= Y_{11}^{\mathrm{MC}} + \mathrm{j}\omega\left(C_{\mathrm{gs}}^{\mathrm{ext}} + C_{\mathrm{gd}}^{\mathrm{ext}}\right) \qquad Y_{12} = Y_{12}^{\mathrm{MC}} - \mathrm{j}\omega C_{\mathrm{gd}}^{\mathrm{ext}} \\ Y_{21} &= Y_{21}^{\mathrm{MC}} - \mathrm{j}\omega C_{\mathrm{gd}}^{\mathrm{ext}} \qquad Y_{22} = Y_{22}^{\mathrm{MC}} + \mathrm{j}\omega\left(C_{\mathrm{ds}}^{\mathrm{ext}} + C_{\mathrm{gd}}^{\mathrm{ext}}\right). \end{aligned} \tag{4}$$

These can be strictly compared with the 'intrinsic' experimental data (extracted from measured S parameters taking away the effect of contact parasitics).

3. Static characteristics

The experimental measurements (curves) and the EMC results (symbols) of the *I–V* characteristics are shown in figure 3. The transfer characteristic for $V_{\mathrm{DS}} = 1.0$ V is shown in the inset. The EMC output characteristics show a very good agreement with the experimental results. In particular, it must be pointed out that the value of the threshold voltage (approximately 0.25 V) is quite well reproduced. Once the main topology parameters of the structure (t_{si}, t_{ox}, L_{ov}, doping profiles, etc) are considered in their real values, the surface oxide charge in the overlap and spacer regions is found to be an important factor in achieving an accurate fit of the simulation results to the experimental extrinsic transconductance (that reaches a maximum value of around 350 S m^{-1} at $V_{\mathrm{DS}} = 1.0$ V), whereas the surface charge in the p-doped layer mainly affects the threshold voltage, having a very small influence on the transconductance. Thus, the surface charge value that allows the best fit of the simulations to the experimental data has been found to be 2×10^{16} m^{-2} in the overlap and spacer regions. With regard to multiplication phenomena, it must be mentioned that impact ionization processes were not observed in the V_{DS} range considered. Since we are interested in studying the behaviour of the device in the saturation regime, the majority of the results shown in this work correspond to $V_{\mathrm{DS}} = 1.0$ V.

The ratio between extrinsic transconductance (g_{m}) and drain current (I_{D}) is an important figure of merit in analogue designs [20, 21]. The transconductance represents the amplification delivered by the device, whereas the drain current represents the power dissipated to obtain such an amplification. Therefore, the $g_{\mathrm{m}}/I_{\mathrm{D}}$ ratio is a quality factor that can be interpreted as a measure of the 'transconductance generation efficiency' [20]. In the case of the FD SOI devices under study, experimental measurements for this parameter in the saturation regime have shown a significantly improved performance compared to that of partially-depleted (PD) SOI and bulk MOSFETs [7]. As can be seen in figure 4, an excellent agreement is obtained between the MC results and the experimental data.

At this point, the EMC method can provide useful information to understand the underlying physics of the device by means of several quantities. This information is also very helpful for the analysis of the SSEC parameters, as we show in section 4. Figure 5 presents the electron concentration under the gate oxide for three different values of V_{GS}, 0.25, 0.75 and 1.25 V, for a drain voltage of 1.0 V. For the lowest value of V_{GS}, the inversion layer begins to appear, showing a peak in the part of the channel nearest to the source region. The device operates in the weak inversion regime, where it is still under cut-off conditions. Over this gate potential, the electron concentration in the inversion layer progressively increases (and so does the length of that inversion layer), and it is able to supply the necessary number of carriers to have a significant flux of current, thus operating in the saturation regime. It must be pointed out that a significant carrier density appears in the source overlap, whereas in the drain side it is practically null, corresponding to a MOSFET device biased in the saturation condition (see figure 3). Nevertheless, for the case of the highest V_{GS} a small concentration appears in the drain side, and the inversion layer extends over the whole channel,

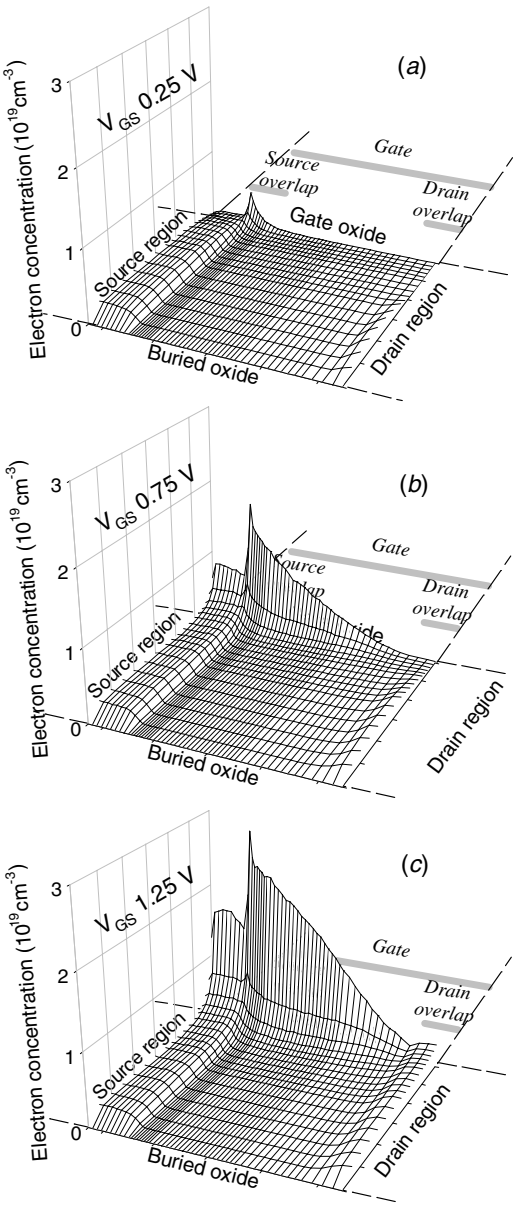

Figure 5. Electron concentration under the gate oxide for three different gate voltages: (*a*) 0.25 V; (*b*) 0.75 V; (*c*) 1.25 V.

which indicates that the device begins to approach the triode region.

Figure 6 shows the electron velocity (figure 6(*a*)) and the electron energy (figure 6(*b*)) for $V_{DS} = 1.0$ V and V_{GS} ranging from 0.5 V to 1.25 V. The profile of electron velocity in the channel is of primary importance in order to analyse non-local effects such as velocity overshoot, which is a well-known short-channel effect in bulk [22] and SOI MOSFETs [23]. For the FD SOI MOSFET under study, an overshoot region is present near the drain end of the channel. The overshoot is less pronounced as the gate voltage is increased. A similar behaviour is detected for the electron energy, a result that has been previously observed in bulk MOSFET devices [11]. This effect is explained by the fact that, for higher gate voltages, the difference between the gate and drain potentials is less significant. As a consequence, there is a reduced electric field at the drain end of the channel, thus lowering both the

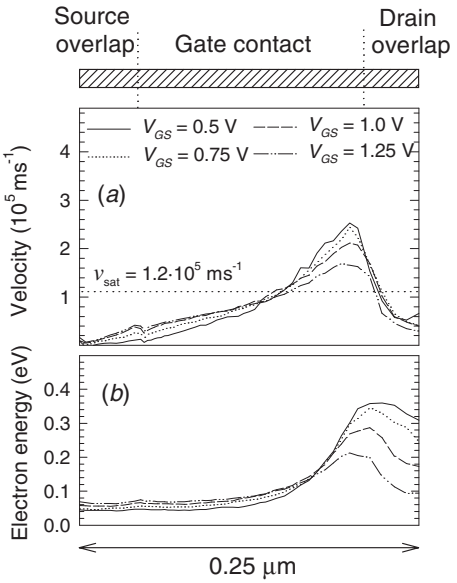

Figure 6. Profiles of velocity (*a*) and energy (*b*) of inversion carriers under the gate oxide for $V_{DS} = 1.0$ V and different gate voltages.

velocity and energy of carriers in that region. It must be remarked that for the lowest gate voltages, values of energy near 0.4 eV are obtained. The presence of these hot electrons can affect the noise behaviour of the device [11] and could even damage the gate oxide at the drain end of the channel, leading to the appearance of traps or surface states at the oxide [3]. Nevertheless, the maximum values of average energy are clearly much lower than the impact ionization threshold energy (1.3 eV), which explains the absence of impact ionization processes in the range of drain voltages considered in our experiments and simulations (below 1.5 V). This absence of impact ionization phenomena, together with the total depletion of holes in the active layer due to the reduced value of the active layer thickness (30 nm) on the FD SOI devices studied, are indicative of a total absence of floating body effects in the bias range considered. This was experimentally confirmed by the fact that the threshold voltage dependence on back gate voltage reaches an almost ideal behaviour [7]. Moreover, experimental results of $1/f$ noise show a kink-free noise behaviour at low frequencies, indicating also the absence of body effects [7, 24].

4. Dynamic response

The knowledge of the SSEC of electronic devices is very helpful in analogue circuitry design. Not only does it allow us to evaluate the dynamic response, but it is also an important step in the calculation of noise parameters. With the aid of EMC numerical simulations, a microscopic physical interpretation of the results can be provided in terms of the spatial profiles of several quantities of interest.

Figure 7 shows the experimental (curves) and simulated values (symbols) for the gate-to-source (C_{gs}), gate-to-drain (C_{gd}) and drain-to-source (C_{ds}) capacitances as a function of V_{GS}. A notable agreement between the EMC results and the experimental data is observed, not only in the range

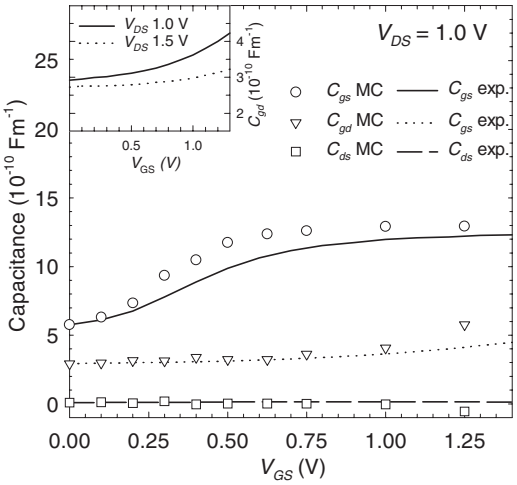

Figure 7. Small-signal equivalent circuit capacitances as a function of gate voltage for $V_{DS} = 1.0$ V. The curves represent the data extracted from experimental measurements, whereas symbols correspond to EMC results. The inset shows the experimental values of C_{gd} as a function of V_{GS} for two different V_{DS} (1.0 and 1.5 V).

of values but also in the bias dependence. The gate-to-source capacitance takes the highest values among the three capacitances in the V_{GS} range considered. For the lowest values of V_{GS}, the concentration of carriers in the inversion layer is not very important yet (the device operates in the depletion regime or in the weak inversion regime; see figure 5), and the capacitance corresponds mainly to the depletion capacitance. As the gate voltage becomes higher, the length of the inversion layer increases notably (and also the number of carriers in that inversion layer, especially near the source end of the channel). As a consequence, C_{gs} also increases. It must be stressed that, from a gate voltage of around 0.75 V, the increase of charge in the source side of the inversion layer is practically linear with V_{GS}. The inversion layer covers the main part of the channel length, and therefore C_{gs} reaches a saturation value. An important result is that a high electron concentration is observed at the overlap region near the source (see figure 5), thus indicating an important weight of the overlap capacitance over the total C_{gs} in this range.

The values of C_{gd} are rather constant with V_{GS} in the whole range considered; only for the highest V_{GS} (from 1.0 V) a tendency to increase is observed. The reason for this slight increment is the appearance of the inversion layer at the drain end of the channel (see figure 5); the depletion in the pinch-off region begins to disappear, and consequently the device would leave the saturation regime for higher gate voltages.

In a bulk MOSFET device, the drain-to-source capacitance may take significant values compared with other SSEC capacitances, which indicates a strong influence of the substrate on the dynamic behaviour of the device [11]. For the FD SOI MOSFET under study, extremely low values for C_{ds} as compared to C_{gd} and C_{gs} are achieved, as figure 7 shows. Therefore, it can be affirmed that by using the FD SOI technology, thanks to the thick buried oxide, the capacitive coupling to the substrate is substantially reduced compared to bulk MOSFETs. This constitutes a key advance in improving the high-frequency behaviour of the device.

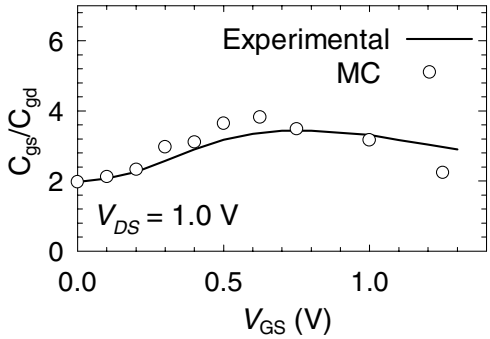

Figure 8. The ratio C_{gs}/C_{gd} versus gate voltage.

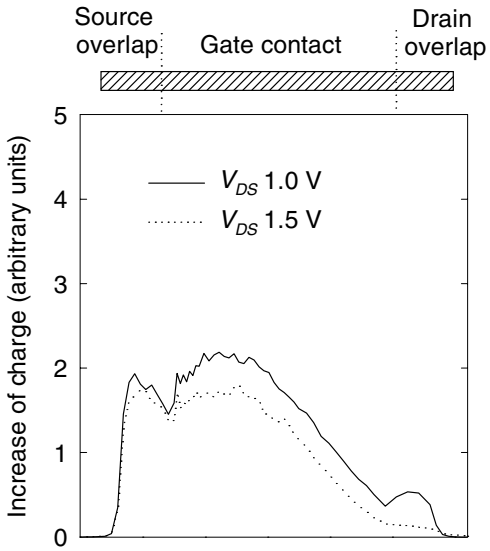

Figure 9. Increase of charge under the gate for two different drain voltages, 1.0 and 1.5 V, and $V_{GS} = 1.0$ V.

The C_{gs}/C_{gd} ratio is a figure of merit of a device. It expresses the ratio between the control capacitance of the active channel (C_{gs}) and the parasitic Miller capacitance (feedback gate-to-drain-capacitance, C_{gd}). High values of this parameter may be indicative of an elevated maximum frequency of oscillation. Figure 8 shows the experimental and simulation results for this parameter as a function of gate voltage. A good agreement is obtained between both. The highest value for the C_{gs}/C_{gd} ratio, 3.5, is obtained for a gate voltage of around 0.7 V.

With regard to the dependence of the SSEC capacitances on V_{DS}, we have observed that in saturation the bias dependence and the values of C_{gs} hardly change with V_{GS} when V_{DS} increases (the maximum EMC values obtained for this capacitance for $V_{DS} = 1.0$ V and $V_{DS} = 1.5$ V are 1290 fF mm^{-1} and 1310 fF mm^{-1}, respectively). This indicates that the C_{gs} capacitance is practically controlled by the gate voltage, provided the device is in the saturation regime. In contrast, the values of C_{gd} decrease when V_{DS} increases, as can be seen in the inset of figure 7, and the dependence with the gate voltage has a lower slope in the case of $V_{DS} = 1.5$ V. To explain this effect, in figure 9 we show the increase of charge under the gate oxide calculated by means of the EMC simulator for $V_{GS} = 1.0$ V and two different drain voltages,

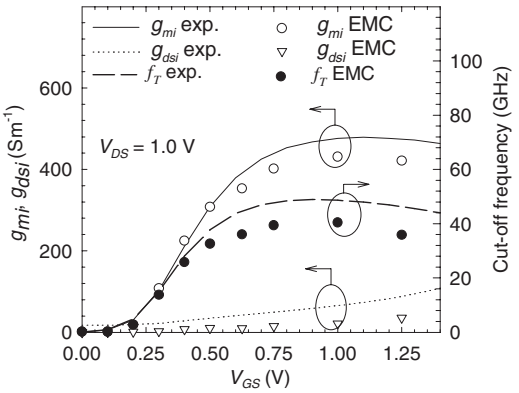

Figure 10. Intrinsic transconductance, output conductance and cut-off frequency as a function of V_{GS} for a drain-to-source voltage of 1.0 V.

1.0 and 1.5 V, when an increment of 0.1 V is applied at the gate. The decrease in C_{gd} with V_{DS} can be associated with the lower increase of charge near the drain for the case of $V_{DS} = 1.5$ V, compared to the case of the lower drain voltage. Therefore, it can be affirmed that in saturation C_{gd} has an important dependence on V_{DS} due to its strong impact on the evolution of the charge at the drain side of the channel, as shown in figure 9.

The experimental data and the simulation results for the intrinsic transconductance, g_{mi}, the intrinsic output conductance, g_{dsi}, and the cut-off frequency, $f_T = g_{mi}/2\pi(C_{gs} + C_{gd})$ [12], are plotted as a function of gate voltage in figure 10 for $V_{DS} = 1.0$ V. The simulation results reproduce accurately the bias dependence of the experimental data for the three parameters, although at high V_{GS} the EMC values of g_{mi} are slightly lower than the experimental measurements, while those of g_{dsi} are, in general, underestimated due to the lower slope of the I_D–V_{DS} EMC characteristics compared to the experimental one. The maximum experimental value for g_{mi} (475 S m^{-1}) is reached for a gate voltage of approximately 1.0 V, but even for $V_{GS} = 0.5$ V a high value (over 300 S m^{-1}) is achieved, which would indicate the capability of the transistor to give a high gain-bandwidth product even for low gate voltages. The maximum value of the cut-off frequency, 48 GHz, is obtained for a gate voltage of 0.8 V. In general, f_T follows the shape of g_{mi}, although for the highest values of gate voltage it tends to decrease, mainly due to the slight increase in the C_{gd} capacitance (figure 7).

5. Conclusions

We have presented an exhaustive experimental and numerical investigation of the static and dynamic characteristics of FD SOI MOSFETs fabricated with a gate length of 0.25 μm. The numerical simulations were performed using a 2D EMC simulator that accurately reproduces the main aspects of the device topology. Furthermore, important real effects, such as surface charges, impact ionization processes or experimental parasitics, have been taken into account. The surface charge at the oxide–semiconductor interface at the overlap and spacer regions was found to be an important parameter to achieve a good fit to the experimental transconductance. The results obtained for the simulated devices are in very good agreement with the experimental measurements, which confirms the validity of the simulator. In particular, we obtain a good description of important design parameters, such as the g_m/I_D ratio.

The velocity overshoot of electrons and the appearance of hot carriers at the drain end of the channel are observed, which are well-known short-channel effects. For a given drain voltage in saturation, the width of the overshoot region and the maximum electron energy decrease as the gate voltage is increased. Impact ionization phenomena were not detected in the studied bias range. This result, together with the complete full depletion of holes in the active layer due to the reduced value of the silicon active film thickness, ensures the absence of floating body effects in the devices under study.

The dependence of the dynamic parameters on the biasing has been analysed by means of the spatial profiles of several relevant quantities, such as local electron concentration, provided by the EMC simulation. With regard to the capacitances, the extremely reduced influence of the capacitive coupling to the substrate that has been found is remarkable, and this is of great interest for high-frequency analogue designs. The C_{gs}/C_{gd} ratio has been also studied, showing the highest values for high V_{DS} in saturation.

In general, the FD SOI MOSFETs studied show a great performance in terms of elevated transconductance and cut-off frequency, which makes them an excellent candidate for rf analogue applications. With regard to the EMC simulator, once it has been validated it constitutes an enormously valuable tool for the optimization of geometrical parameters and the analysis of the static, dynamic, and noise device performance when the gate length is scaled down. This will be the subject of forthcoming works.

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References

[1] Iwai H 1998 *Microelectron. J.* **29** 671
[2] Schaeffer D K and Lee T H 1997 *IEEE J. Solid-State Circuits* **32** 745
[3] Colinge J P 1997 *Silicon-on-Insulator Technology: Materials to VLSI* 2nd edn (Norwell, MA: Kluwer)
[4] Cristoloveanu S 2001 *Solid-State Electron.* **45** 1403
[5] Jacoboni C and Lugli P 1989 *The Monte Carlo Method for Semiconductor Device Simulation* (Berlin: Springer)
[6] Raynaud C *et al* 2000 *Proc. 30th European Microwave Week GAAS'2000* p 268
[7] Vanmackelberg M *et al* 2002 *Solid-State Electron.* **46** 379
[8] Goffioul M, Raskin J P and Vanhoenacker-Janvier D 2000 *Proc. 30th European Microwave Week GAAS'2000* p 407
[9] Mateos J, González T, Pardo D, Hoël V and Cappy A 2000 *IEEE Trans. Electron Devices* **47** 1950
[10] Martín -Martínez M J, Pérez S, Pardo D and González T 2001 *J. Appl. Phys.* **90** 1582
[11] Rengel R, Mateos J, Pardo D, González T and Martín M J 2001 *Semicond. Sci. Technol.* **16** 939
[12] Tsividis Y P 1999 *Operation and Modeling of the MOS Transistor* (Boston: McGraw-Hill)

[13] Kane E O 1967 *Phys. Rev.* **159** 624
[14] Lee C, Logan R, Batdrof R, Kleimack J and Wiegmann W 1964 *Phys. Rev.* **134** A761
[15] Woods M, Johnson W and Lampert M 1973 *Solid-State Electron*. **16** 583
[16] González T and Pardo D 1995 *IEEE Trans. Electron Devices* **42** 605
[17] Berroth M and Bosch R 1990 *IEEE Trans. Microwave Theory Technol*. **38** 891
[18] Dambrine G, Cappy A, Heliodore F and Playez E 1988 *IEEE Trans. Electron Devices* **32** 1151
[19] Dambrine G, Raskin J P, Danneville F, Vanhoenacker-Janvier D, Colinge J P and Cappy A 1999 *IEEE Trans. Electron Devices* **46** 1733
[20] Silveira F, Flandre D and Jespers P G A 1996 *IEEE J. Solid-State Circuits* **31** 1314
[21] Colinge J P 1998 *IEEE Trans. Electron Devices* **45** 1010
[22] Laux S E and Fischetti M V 1988 *IEEE Electron Device Lett.* **9** 467
[23] Cheng B, Rao R and Woo J C S 1999 *IEEE Electron Device Lett*. **20** 538
[24] Tseng Y-C *et al* 1999 *IEEE Trans. Electron Devices* **46** 1685