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Dynamic Monte Carlo study of isolated-gate InAs/AlSb HEMTs

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Abstract

In this work, by means of Monte Carlo simulations, the static and dynamic behavior of isolated-gate InAs/AlSb high electron mobility transistors (Sb-HEMTs) has been studied and compared with experimental results. The influence of the existence of a native oxide under the gate, the value of the surface charges in the gate recess and the possible variation of electron sheet carrier density, n_s , have been studied. A decrease in the gate-source capacitance, transconductance and intrinsic cutoff frequency is observed because of the presence of the native oxide, while changes in the value of the surface charges in the recess only introduce a threshold voltage shift. The increase of n_s shifts the maximum of the transconductance and intrinsic cutoff frequency to higher values of drain current and improves the agreement with the experimental results.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The search for improved cutoff frequencies in high electron mobility transistors (HEMTs) pursued by increasing the In content in the channel of 'traditional' InGaAs/InAlAs HEMTs suggests the relevance of a new generation of HEMTs based on the InAs/AlSb heterojunction (Sb-HEMTs) [1–4]. The very high mobility of the channel material (InAs), along with the strong confinement of the electrons in the channel due to the large offset in the conduction band ($\Delta E_c = 1.35$ eV) of the InAs/AlSb heterostructure, allows the Sb-HEMT to achieve the high-frequency, low-noise and low-power requirements demanded for radio-astronomy receivers, passive imaging and satellite communications [5, 6].

One of the most important challenges in the development of Sb-HEMTs is to achieve a decrease of the large gate leakage current of these devices. For this sake, a possible approach is to avoid the oxide-removal step after the recess etching in the fabrication process, favoring the appearance of a native oxide under the gate [7]. The theoretical study of the macroscopic consequences of introducing

this native oxide and also the physical understanding of the internal microscopic behavior of the device are essential tasks in the development and optimization of Sb-HEMTs.

Due to the very high mobility of the InAs channel, electron transport can become ballistic or at least quasi-ballistic, thus making Monte Carlo (MC) simulations the most accurate modeling technique as compared with other approaches like drift diffusion or hydrodynamic methods. Moreover, MC simulations provide not only the static characteristics and relevant physical information inside the devices but also their dynamic and noise behavior.

In this work we present the results of MC simulations able to correctly reproduce experimental measurements, at low V_{ds} before the onset of impact ionization, of the static behavior and small-signal equivalent circuit of isolated-gate Sb-HEMTs. The influence of the native oxide and the associated surface charges in the gate recess, and the variation of n_s have been studied, thus providing valuable information for the optimization of the devices.

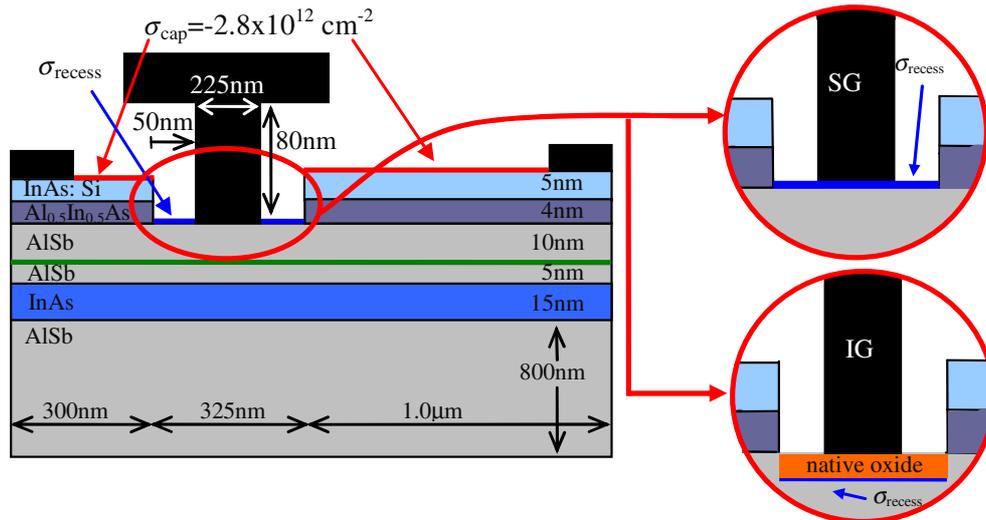


Figure 1. Scheme of the simulated devices.

2. Device description and simulation model

The active layer for the fabricated isolated-gate Sb-HEMT [6, 7] is composed of an AISb buffer of 800 nm followed by an InAs channel of 15 nm and a 15 nm thick AISb barrier, a 4 nm protection layer of $\text{In}_{0.5}\text{Al}_{0.5}\text{As}$ and a 5 nm highly Si doped InAs cap ($N_D = 5 \times 10^{18} \text{ cm}^{-3}$) on top. Electrons are introduced by a δ -doping of $\delta = 4.5 \times 10^{12} \text{ cm}^{-2}$, 5 nm far from the channel. To fabricate the 225 nm gate Sb-HEMTs ($2 \times 50 \mu\text{m}$ wide), the mesa isolation was performed by a chlorine-based dry etching method, then Pd/Pt/Au ohmic contacts were evaporated and annealed, and the T-shaped gate was formed by a tri-layer resist stack defined with electron beam lithography. The recess etching, using citric acid, stops at 9 nm distance from the surface (the top of the AISb Schottky layer). The typical oxide-removal step after the recess etch step has not been performed for these devices, thus favoring the appearance of a native oxide under the gate that decreases the large leakage current of InAs-based HEMTs [7].

A semiclassical ensemble MC simulator self-consistently coupled with a two-dimensional Poisson solver has been used for device simulations [8, 9]. The simulator is properly adapted to work with narrow-band-gap channel HEMTs [10]. As seen later, impact ionization becomes crucial for $V_{ds} > 0.3 \text{ V}$. We will focus on lower voltages (where the dynamic and noise performances are expected to be optimal). Hence, impact ionization has not been considered due to the complications introduced in the calculation of the small-signal equivalent circuit [11]. We study impact ionization processes and the consequent kink effect in a separate work dealing only with the static behavior of the transistors [12].

The simulated 225 nm gate Sb-HEMT is shown in figure 1. In order to decrease the number of simulated particles and reduce the simulation time, the ohmic source-recess region has been shortened from the experimental value of around $1.0 \mu\text{m}$ to 300 nm. The omitted part can be introduced later as a contribution to the external source resistance [8]. To reproduce the surface charges that appear in the semiconductor–air

interface, we have included a surface charge density $\sigma_{\text{cap}}/e = -2.8 \times 10^{12} \text{ cm}^{-2}$, e being the electron charge (value that reproduces the experimental sheet electron density in the channel, $n_s = 2.1 \times 10^{12} \text{ cm}^{-2}$ [7]). The negative surface charge at the recess floor, σ_{recess} , may be different from the one at the top of the cap layer [8] since it depends on the etching process and the material is different. Moreover, the value assigned to σ_{recess} also accounts for the possible presence of charges within the native oxide. Therefore, this parameter will be taken as adjustable, within reasonable values.

AISb oxidation is a complex process [13], as it is difficult to know the composition of the oxide and its thickness. The static and dynamic behaviour of the devices has been simulated, analyzing the influence of the dielectric constant and oxide thickness. We have observed that increasing the dielectric constant is equivalent to decreasing the oxide thickness, obtaining a reasonable agreement with experimental data considering a 2 nm thick oxide with a dielectric constant of 2.2 (corresponding to aluminum hydroxide).

Three different cases have been simulated in order to study the intrinsic influence of the native oxide and the surface charges at the bottom of the recess (figure 1):

- Device without native oxide under the gate and with a surface charge on the recess $\sigma_{\text{recess}}/e = -1.2 \times 10^{12} \text{ cm}^{-2}$. We will call it Schottky-gate (SG) Sb-HEMT.
- Device with the same σ_{recess} as the SG, but with a 2 nm thick oxide with dielectric constant 2.2 under the gate. We will call it isolated-gate (IG) Sb-HEMT.
- Device identical to IG but with a higher negative surface charge at the bottom of the recess $\sigma_{\text{recess}}/e = -2.8 \times 10^{12} \text{ cm}^{-2}$ (IG2).

3. Results

3.1. Static characteristics

In order to compare the intrinsic MC results with the extrinsic experimental ones, there are two considerations. First, we

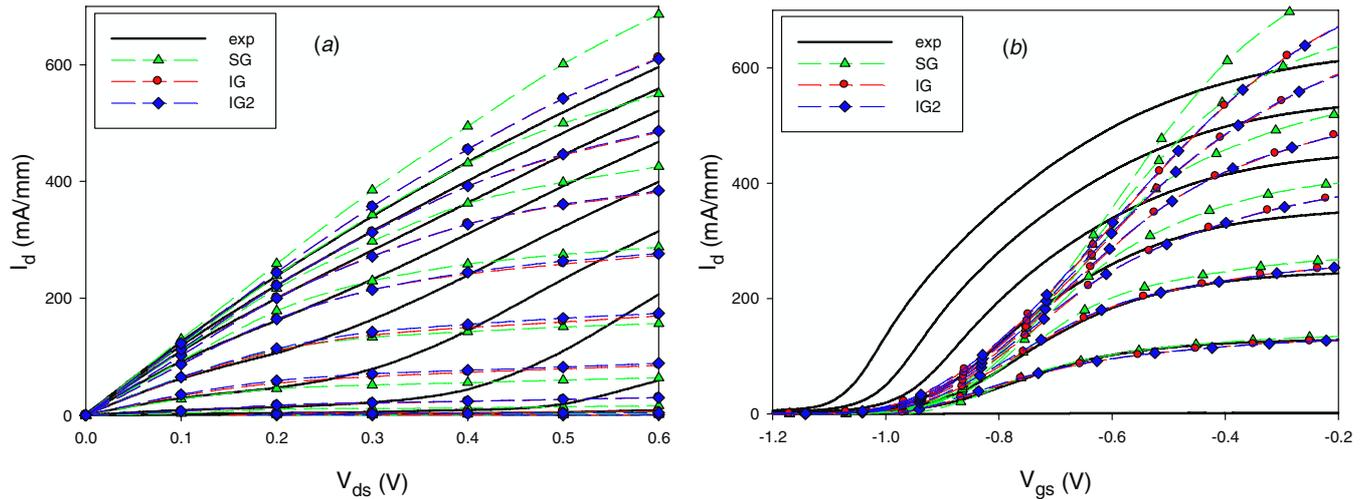


Figure 2. Comparison of the experimental (black solid lines) and MC (symbols, dashed colored lines) results: green triangles for SG, red circles for IG and blue diamonds for IG2 HEMTs. (a) I_d - V_{ds} from $V_{gs} = -1.15$ to -0.45 V, step 0.1 V and (b) I_d - V_{gs} from $V_{ds} = 0.1$ to 0.6 V, step 0.1 V.

have to introduce the effect of the parasitic elements which are not present in our simulations. Consequently, source and drain contact resistances R_s and R_d have been included for a proper fitting of the IG case. The best fit was found with $R_s = 0.13 \Omega \text{ mm}$ and $R_d = 0.38 \Omega \text{ mm}$, in good agreement with the experimental values of the contact access resistances. The second post-processing step to be done with the intrinsic MC results is a V_{gs} shift (ΔV_{gs}) associated with the gate properties. In the case of the SG Sb-HEMTs, this is due to the metal–semiconductor Schottky barrier height, which is not considered in the simulations. This should introduce a positive shift of V_{gs} with respect to the electrical bias applied in the MC simulations. However, in this case the ΔV_{gs} needed to correctly reproduce the experimental threshold voltage has a negative value (-0.37 V). This fact confirms the presence of the native oxide in the IG Sb-HEMT. This is also the reason why the reference case of the MC simulations used in the comparison with the experimental results is the IG-HEMT. In the cases IG and IG2, the ΔV_{gs} introduced is attributed to the effect of (i) the metal–semiconductor workfunction difference, (ii) the surface charges at the semiconductor–oxide interface and (iii) the volume charges within the oxide, whose global value is not known. The best fit for IG and IG2 is achieved with a V_{gs} shift of 0.03 V and -0.27 V, respectively. The different ΔV_{gs} just compensates the effect of the higher σ_{recess} in IG2 with respect to IG, which results that (in this range of values) σ_{recess} has almost no influence on the dc and the dynamic behavior of the devices, so that we have some flexibility for choosing its value in the MC simulations. In the SG case, the V_{gs} shift does not have a physical meaning, but it has been kept in order to perform an understandable comparison of the different simulated devices.

In figure 2, a good agreement between MC simulations of Sb-HEMTs and experimental results for low V_{ds} (up to 0.2–0.3 V) is shown, when impact ionization mechanisms are not frequent, especially in the case of IG and IG2. For higher V_{ds} , a very high output conductance resulting from

impact ionization appears in the experimental output I - V curves, figure 2(a), with a subsequent threshold voltage shift in the transfer characteristics, figure 2(b), not reproduced by the simulations. Figure 2 shows that IG and IG2 provide nearly the same dc results since the variation of the value of σ_{recess} only results in a different threshold voltage (that is compensated by the difference in the ΔV_{gs} used to adjust the MC characteristics) without much affecting the final shape of the I - V curves. It can also be observed that the absence of oxide under the gate (SG case) somewhat increases the drain current as a consequence of a better charge control by the gate. This is the penalty that the IG design pays for the reduction of the gate leakage current. Note that the gate current is not shown in the simulations since it cannot be calculated with our semiclassical MC model.

3.2. Dynamic results

The simulated and experimental results for the intrinsic small-signal equivalent circuit parameters of the SG and IG HEMTs are compared in figure 3 for $V_{ds} = 0.2$ V, where impact ionization is negligible and the optimum noise conditions are experimentally reached [6]. The MC results have been obtained from the admittance parameters extracted by the Fourier analysis of the response of the transistor currents to voltage steps applied at the gate and drain contacts [14]. In order to perform a correct comparison between the intrinsic experimental and simulated equivalent circuits, we have to consider that even when de-embedding the extrinsic parameters from the experimental results, there are still some effects that the MC is not accounting for, such as fringing and cross talk capacitances in the layout. Indeed, three extrinsic capacitances, C_{gs}^{extr} , C_{gd}^{extr} and C_{ds}^{extr} , have been added to the MC results to reproduce the effects associated with the topology of the devices (see [14] for a more detailed explanation). The values of C^{extr} have been obtained by fitting the experimental data at zero current ($C_{ds}^{\text{extr}} = 120 \text{ fF mm}^{-1}$, $C_{gd}^{\text{extr}} = 120 \text{ fF mm}^{-1}$,

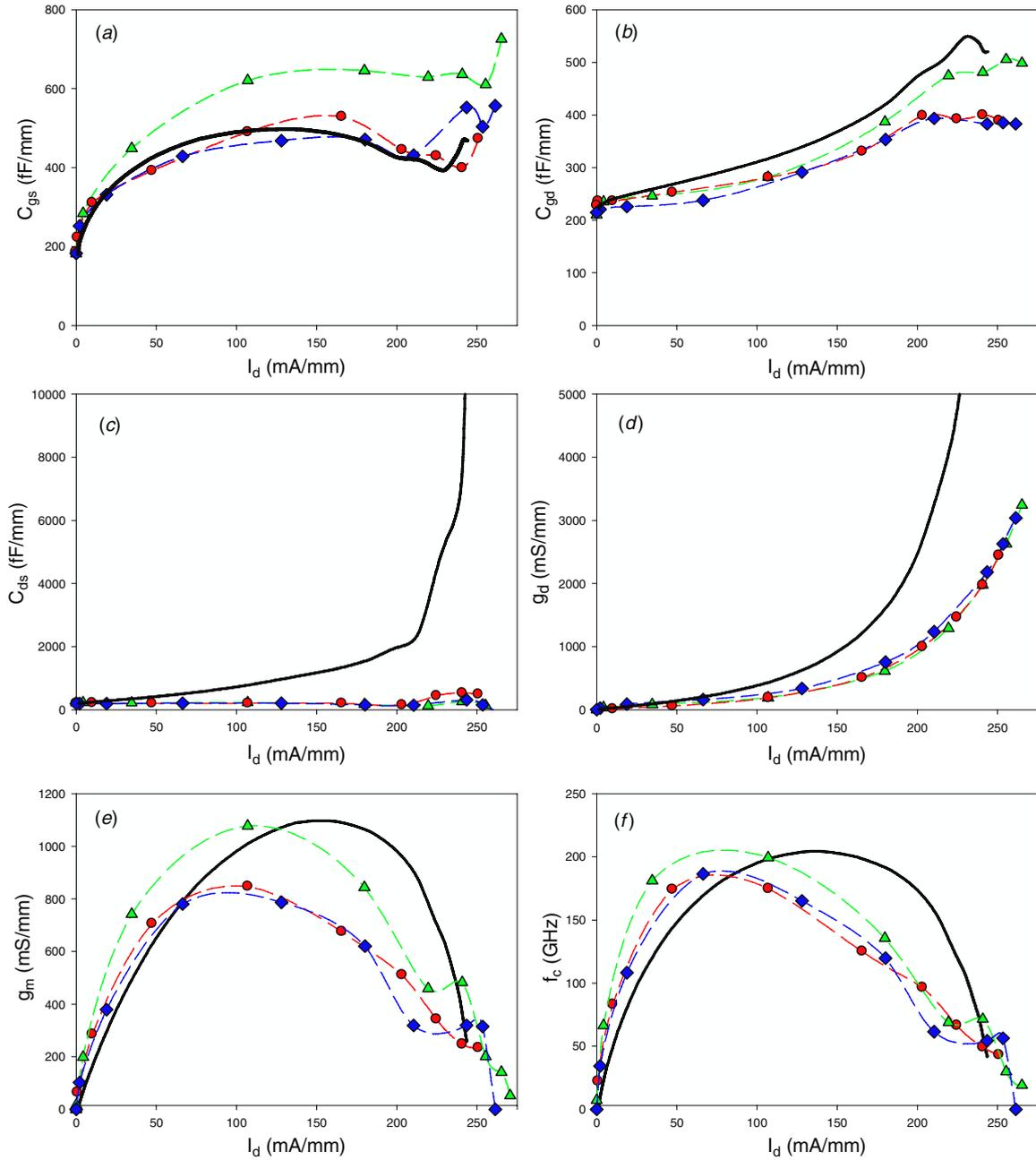


Figure 3. Comparison between the values of the (a) gate-source, C_{gs} (b) gate-drain, C_{gd} , and (c) drain-source, C_{ds} , capacitances, and (d) drain conductance, g_d , (e) transconductance, g_m , and (f) intrinsic cutoff frequency $f_c = g_m/2\pi(C_{gs} + C_{gd})$ measured in the fabricated HEMT (black line) and obtained by MC simulations for the SG (green triangles), IG (red circles), and IG2 (blue diamonds) cases as a function of I_d for $V_{ds} = 0.2$ V.

$C_{gs}^{extr} = 10 \text{ fF mm}^{-1}$), where only the effect of the geometric capacitances remains, which are independent of the applied bias.

The intrinsic equivalent circuit combined with C^{extr} is compared in figure 3 with the intrinsic experimental small-signal equivalent circuit. The simulated IG and IG2 cases are very similar, thus confirming that the surface and volume charges below the gate produce only a threshold voltage shift without influencing the dynamic behavior of the devices. These two simulated cases (IG and IG2) provide better agreement with the experimental results for C_{gs} than the SG

one, while for C_{gd} the gate oxide does not have a strong influence (figures 3(a), (b)). The increased value of both C_{gs} and C_{gd} in the SG case is consistent with the increased gate-channel capacitance in the absence of the gate oxide.

The existence of a frequency dependence in the experimental results of C_{ds} and g_d causes considerable disagreement between the experimental and MC results observed in figures 3(c) and (d). We attribute this frequency dispersion to the existence of holes in the buffer whose response time is quite slow. This effect has already been observed in InGaAs HEMTs [11, 15], even under biases

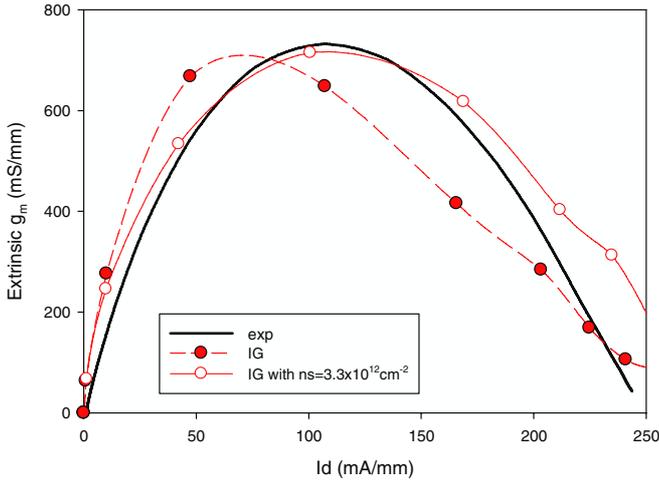


Figure 4. Extrinsic g_m calculated through equation (1) for $V_{ds} = 0.2$ V for the fabricated HEMT (black solid line) as a function of I_d compared with the IG MC results for two different σ_{cap} values leading to $n_s = 2.1 \times 10^{12} \text{ cm}^{-2}$ (red circles, dashed red line) and $n_s = 3.3 \times 10^{12} \text{ cm}^{-2}$ (white circles, solid red line).

where the kink effect is still not apparent in the I - V curves. When holes are accumulated, g_d shows a frequency dispersion associated with their accumulation time (related to impact ionization processes and the time which holes take to move from the region where they are generated to the accumulation zone).

The presence of the gate oxide reduces g_m in the IG with respect to the SG device (figure 3(e)), as expected from the inferior charge control shown in figure 2. Consequently, a decrease is also observed in the intrinsic cutoff frequency $f_c = g_m / 2\pi(C_{gs} + C_{gd})$ for the IG cases. f_c is plotted in figure 3(f). The lower g_m is partially compensated by a decrease of C_{gs} .

For the IG cases in figure 3(e), the maximum intrinsic g_m and the drain current are lower in the MC simulations than for the experimental curve. This disagreement was unforeseen mainly because much better agreement exists when the extrinsic g_m is extracted from the static I - V curves (figure 2, IG case). Indeed, the values for the contact resistances to be added to MC simulations were chosen in order to obtain the best fit for the extrinsic I - V characteristics. This inconsistency can be explained by the discrepancy in the drain conductance (figure 3(d)) since g_m^{extr} and g_m^{intr} are coupled by the relation

$$g_m^{\text{extr}} = \frac{g_m^{\text{intr}}}{(1 + g_m^{\text{intr}} R_S)[1 + g_d^{\text{intr}}(R_S + R_d)]}. \quad (1)$$

In fact, the extrinsic g_m obtained using equation (1), plotted in figure 4, shows that the maximum values of the IG MC and experimental extrinsic g_m are similar, even if the shape of the curve is not really the same (the peak is found at lower currents in the simulations). In order to better reproduce the experimental results, we have considered another possible source of discrepancies between the experimental and simulated results, which is the variation of the value of the sheet electron density in the channel. The results of Hall measurements used in MC simulations were obtained in the epitaxial structure before device processing.

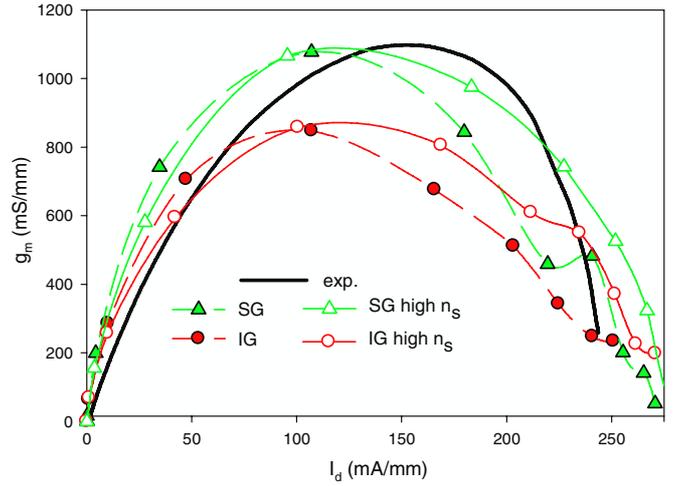


Figure 5. Intrinsic g_m for $V_{ds} = 0.2$ V for the fabricated HEMT (black solid line) as a function of I_d compared with the MC intrinsic results, SG (triangles) and IG (circles), for the two values of n_s considered ($n_s = 2.1 \times 10^{12} \text{ cm}^{-2}$ colored symbols, dashed lines; $n_s = 3.3 \times 10^{12} \text{ cm}^{-2}$ white symbols, solid lines).

During device processing, the value of n_s may be affected. A higher sheet electron density ($n_s = 3.3 \times 10^{12} \text{ cm}^{-2}$) has been achieved in our simulations by means of the consideration of a lower value for $\sigma_{cap}/e = -1.5 \times 10^{12} \text{ cm}^{-2}$. However, this just affects the source and drain access regions and not the active part of the device, thus decreasing the source and drain access resistances due to the higher n_s on those regions (the electron density under the recess and the gate practically do not change). However, we have to note here that the values for the extrinsic resistances added to all the intrinsic MC simulations have been kept constant, so that the total contact resistance decrease would be even higher.

Figure 4 shows that the peak in g_m is shifted to higher I_d when n_s is higher, thus providing much better agreement with the experimental values. The same trend is followed by the intrinsic g_m , as can be observed in figure 5, where the comparison between the SG and IG MC cases with the two values of n_s (2.1×10^{12} and $3.3 \times 10^{12} \text{ cm}^{-2}$) is shown. If we focus on the IG MC simulation, the decrease of the source and drain access resistances due to the higher n_s also leads to a slight reduction in the values of C_{gs} , while those of C_{gd} remain similar, as shown in figure 6. The slight decrease of C_{gs} (while C_{gd} remains practically constant) is the result of a complex bi-dimensional electrostatic effect, resulting from the influence of σ_{cap} at the lateral parts of the active region of the device (mainly at the source side). This is the result of a bi-dimensional electrostatic effect, resulting from the influence of σ_{cap} in the lateral parts of the active region of the device (mainly at the source side).

In order to discern the importance of each of the studied parameters on the extrinsic high-frequency performance of the devices, figure 7 shows the extrinsic current gain cutoff frequency, f_t , estimated as [16]:

$$f_t = \frac{g_m^{\text{intr}}/2\pi}{(C_{gs} + C_{gd})[1 + g_d^{\text{intr}}(R_S + R_d)] + C_{gd}g_m^{\text{intr}}(R_S + R_d)}. \quad (2)$$

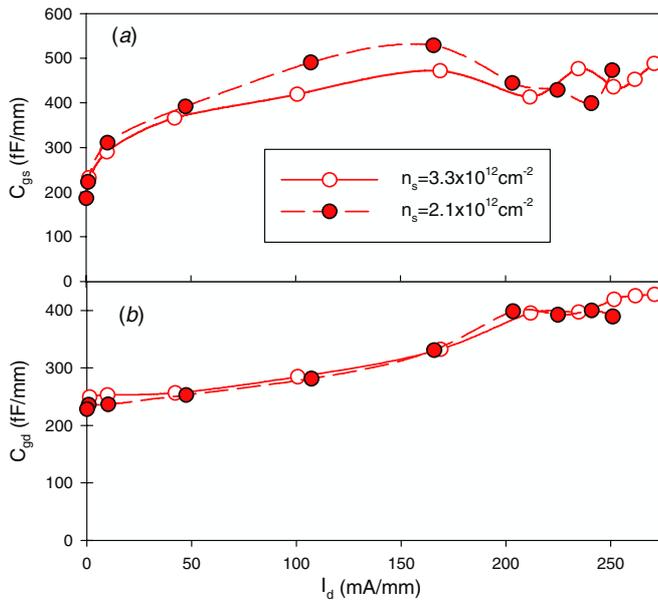


Figure 6. Comparison between the intrinsic values of the (a) gate-source, C_{gs} , and (b) gate-drain, C_{gd} , capacitances obtained by MC simulations of the IG device for the two values of n_s considered: $n_s = 2.1 \times 10^{12} \text{ cm}^{-2}$ (colored red circles, dashed lines) and $n_s = 3.3 \times 10^{12} \text{ cm}^{-2}$ (white circles, red solid lines) as a function of I_d for $V_{ds} = 0.2 \text{ V}$.

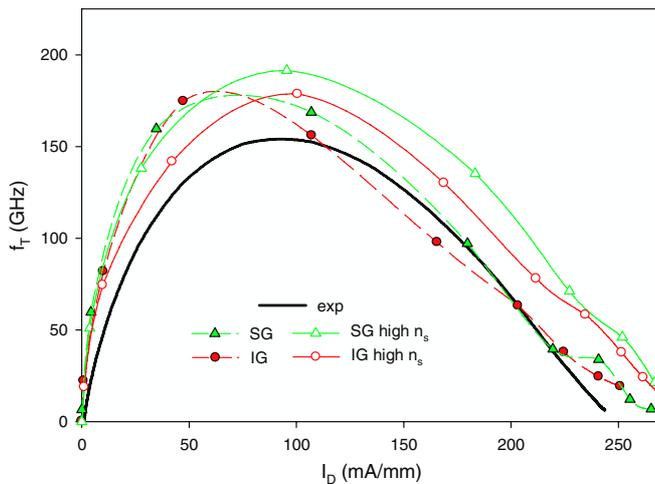


Figure 7. f_t estimated through equation (2) as a function of I_d for $V_{ds} = 0.2 \text{ V}$ in the fabricated HEMT, compared with the SG and IG MC results with two different values of n_s .

Not many differences are found between the f_t values obtained for the IG and SG cases, thus showing that a thin gate oxide helps to reduce the gate leakage current without much degrading the high-frequency performance of the HEMTs. On the other hand, an increased value of n_s causes the peak f_t to be shifted to higher I_d (and to slightly increase its value) in a similar way as happened with g_m , providing reasonable agreement with the experimental results. The lower experimental values of f_t with respect to the MC ones are mainly due to the discrepancy in the g_d values.

4. Conclusions

The static and dynamic behavior of InAs/AlSb isolated-gate Sb-HEMTs has been studied by MC simulations and compared with experimental results, with which reasonable agreement has been obtained for $V_{ds} < 0.3 \text{ V}$, when impact ionization processes are not frequent. Discrepancies arise for g_d and C_{ds} at high drain current due to the frequency dispersion of the experimental measurements, that we attribute to the presence of holes in the buffer originated by impact ionization in the InAs channel. This, added to the relation between the intrinsic and extrinsic g_m , where g_d is involved, makes the simulated intrinsic dynamic g_m values depart from the experimental ones for high I_d , while the static extrinsic g_m is well reproduced.

We have shown that the native oxide under the gate used to reduce the gate leakage current leads to a decrease in g_m , due to the expected poorer channel charge control by the gate, and also in C_{gs} and f_c , but it does not degrade significantly the extrinsic high-frequency performance of the IG HEMTs (estimated through f_i).

When different values for the surface charges at the bottom of the recess of the IG HEMTs are used in the simulation, only a threshold voltage shift is observed in both static and dynamic characteristics, meaning that there is some flexibility for the choice of this MC parameter. When increasing the n_s value in the MC simulations, better agreement with the experimental shape of g_m and f_i is obtained (the maximum shifts toward higher I_d), thus indicating the possibility that the sheet electron density in the channel of the Sb-HEMTs was modified during the device processing.

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